Memorias del Congreso Nacional de Control Automático
ISSN: 2594-2492

Generalized Model-Based Controller for 3-Phase CHB-nL Converters in Power Filter Applications

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Abstract: This research paper aims to address a control methodology for a 3-phase cascaded H-bridge (CHB) converter, in the general case of n-levels (CHB-nL). The proposed method is used not only to eliminate the harmonic currents caused by non-linear loads, but also to compensate reactive power. For these goals, the generalized model of the CHB-nL converter is first introduced by including the effect of the line impedance. The control objectives are defined in terms of current tracking, and voltage balance and regulation in all H-bridges. Then the suggested controller must guarantee tracking of the line current towards an appropriately defined reference by an inner control loop. In the proposed approach, the current reference is selected to be proportional to the line voltage. The proposed controller also includes outer voltage loops to guarantee regulation and balance of the involved capacitor voltages. The accuracy and performance of the proposed controller are evaluated in simulation under load variations and unbalance conditions during the startup period and steady-state stage.

Keywords: Current harmonics, multilevel converter, CHB converters, active power filters, PBC controller.

1. INTRODUCTION

Industrial loads introduce a significant amount of harmonics into the power system network. These harmonics increase the losses and reduce the lifetime of the power system equipments. Hence, it is of vital importance to control the injection of these harmonics into the electrical network. Active Power Filters (APF), is one of the best solutions to the latter objective (Valdez et al., 2013). The APF is roughly a new type power electronics equipment, which can not only filter harmonics but also compensate reactive power. Furthermore, APFs have a reasonable performance price ratio. System impedance does not influence the characteristic of harmonic restraint by APF (Wang , 2009). These filters can be implemented using different multilevel converter topologies whose basic forms are: Diode-Clamped Multilevel Converter (NPC), Flying-Capacitor Multilevel Converter (FCC) and Cascade H-Bridge (CHB) converter. All of these topologies have demonstrated that they can meet the growing demand of power quality associated with reducing harmonic distortion and electro-magnetic interference (EMI) through synthesizing the AC output voltage in various levels, where the obtained staircase waveform is equivalent to the sinusoidal waveform. Moreover, the multilevel converters have the ability to increase the magnitude of the output voltage, and since they are composed of the cascade connection of several semiconductor devices that operate at a lower switching frequency, they reduce voltage stresses between the connected devices. This phenomenon can lead to a reduction of switching losses, which represents an increment in efficiency. This work employs the CHB multilevel converters due to its modularity, and adjustment of the quality of the output voltage in the converter (Rashid , 2002), (Gultekin , 2012),(Kouro et. al., 2011).

A variety of current control methods for APFs has been introduced in the literature for obtaining the APF compensation currents. These methods among others, are hysteresis control, predictive control, resonant control, instantaneous reactive power theory, and repetitive control (Monteiro et el., 2007), (Hinduja et el., 2015). In (Valdez et al., 2015) and (Peréz et al., 2016), a procedure relies on passivity-based control (PBC) is reported, in which the dynamic system is considered as sum of the energy transformation subsystems, where the controller is designed to regulate the energy exchanges between the system and its environment. This process, reshapes the energy of the closed-loop system, and an additional damping is included to guarantee convergence towards the desired equilibrium point.

The present research work stands as an extension to the single-phase control methodology proposed in our previous work (Valdez et al., 2015), in order to be suitable for the 3-phase CHB converter in general case of n-levels (CHB-nL). In fact the this research also plays part as an improvement to the 3-phase control technique detailed in (Peréz et al., 2016), where a particular case of 5-level CHB converter was studied. The proposed extended version is then validated based on numerical simulations that consider a dynamical test under load perturbations and unbalance conditions.

The rest of the paper is organized as follows: Section 2 provides a brief description of the 3-phase CHB-nL converter under study, and introduces the corresponding mathematical model, while the proposed extension of the controller scheme is detailed in Section 3; Section 4 shows

the evaluation of the proposed control methodology in a 3-phase CHB topology with seven-levels (CHB-7L); Finally the conclusions are described in Section 5.

2. 3-PHASE CHB-nL CONVERTER

Figure 1 illustrates the general standard structure of the 3-phase CHB-nL used as shunt APF (SAPF) system connected to the grid, where a 3-phase power supply v_{Gp} whose fundamental frequency is f_0, with $p \in \{1,2,3\}$ representing a particular phase, feeds a non-linear (NL) distorting load. Without a loss of generality, in this work, the NL is assumed a non-controlled full bridge rectifier with and a resistive load R_0. The 3-phase CHB-nL, which is built by a cascade arrangement of N H-bridges per phase is attached in parallel to the load in the point of common coupling (PCC) through an inductor filter L. The grid voltages measured at PCC are denoted as v_{Sp}, and r_G and L_G are the resistance and inductance of the source impedance, respectively. Notice that the SAPF is connected in such a way that it injects current to directly cancel the distorted currents.

2.1 Mathematical Model

According to the studied topology illustrated in Fig 1, the analysis of the mathematical model can be divided into current and voltage dynamics, as discussed next.

2.1.1 Current Dynamics

Kirchhoff's laws can be applied in order to obtain the generalized mathematical model that describes the system represented in Fig. 1. This process yields the following expressions,

$$(L+L_G)\frac{d}{dt}i_{Sp} = v_{Gp} - r_G i_{Sp} - v_p - v_{Z0} + L\frac{d}{dt}i_{0p} \quad (1)$$

$$i_{Sp} = i_p + i_{0p}, \qquad p \in \{1,2,3\} \quad (2)$$

where v_{Z0} is the voltage between points Z and 0; i_{Sp} are the grid currents. i_{0p} are the distorting load currents, and i_p are the injected currents; Furthermore, if we define

$$v_{pj} = v_{Cpj}u_{pj}, \quad (3)$$

as the output voltage of each single H-bridge converter, then the sum of the output voltages within the whole p-phase can be expressed as

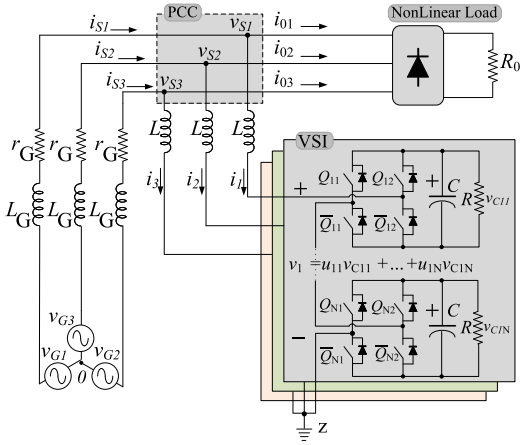

Fig. 1. *3-phase CHB-nL converter used as SAPF.*

$$v_p = \sum_{j=1}^{N} v_{Cpj}u_{pj} = \sum_{j=1}^{N} v_{pj}, \quad j \in \{1,2\cdots,N\}. \quad (4)$$

with N a total number of bridges per phase; v_{Cpj} the capacitors voltages on the DC buses; parameters L and C are the filter inductance and the capacitance of DC buses, respectively; the losses have been modeled as simple resistors R in parallel to the DC capacitors; u_{pj} denote the switch position functions for each H-bridge. The later variables represent the actual control inputs taking values in the discrete set $\{-1,0,1\}$. In brief, each single H-bridge converter works as follows: Within any p-phase and j-th H-bridge, if $u_{pj} = 1$, transistors Q_{j1} and $\bar{Q}_{j2}$ are turned *ON*, while transistors $\bar{Q}_{j1}$ and Q_{j2} are in *OFF* state. The opposite happens for $u_{pj} = -1$. Moreover, for $u_{pj} = 0$, the pair (Q_{j1},Q_{j2}) or ($\bar{Q}_{j1}$,$\bar{Q}_{j2}$) is switched *ON*.

Since this research work considers an averaged model then the switch positions u_{pj} will represent, from now on, duty cycles, i.e., continuous signals taking values in the interval $[-1,1]$ because, in a real implementation, a relatively high (effective) switching frequency is considered together with an appropriate modulation technique.

Next, assuming that the voltage source is balanced and free of harmonic contaminations, i.e.

$$v_{G1} + v_{G2} + v_{G3} = 0,$$
$$i_{S1} + i_{S2} + i_{S3} = 0.$$

These suppositions yields

$$v_{Z0} = -\frac{1}{3}\left(v_1 + v_2 + v_3\right). \quad (5)$$

Taking (5) into (1) and organizing, results in

$$(L+L_G)\frac{d}{dt}\mathbf{i}_S = \mathbf{v}_G - r_G\mathbf{i}_S - \mathbf{B}\mathbf{v} + L\frac{d}{dt}\mathbf{i}_0, \quad (6)$$

with $\mathbf{i}_S = [i_{S1} \;\; i_{S2} \;\; i_{S3}]^\intercal$, $\mathbf{v}_G = [v_{G1} \;\; v_{G2} \;\; v_{G3}]^\intercal$, $\mathbf{i}_0 = [i_{01} \;\; i_{02} \;\; i_{03}]^\intercal$, $\mathbf{v} = [v_1 \;\; v_2 \;\; v_3]^\intercal$ a vector of the sum of converter output voltages within the whole p-phase, and

$$\mathbf{B} = \tfrac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}.$$

The proposed frame work requires the transformation of (6) into $\alpha\beta$-coordinates as follows

$$L\frac{d}{dt}\mathbf{T}\mathbf{i}_S = \mathbf{T}\mathbf{v}_G - r_G\mathbf{T}\mathbf{i}_S - L_G\frac{d}{dt}\mathbf{T}\mathbf{i}_S - \mathbf{T}\mathbf{B}\mathbf{T}^{-1}\mathbf{v}_{\alpha\beta} + L\frac{d}{dt}\mathbf{T}\mathbf{i}_0,$$

$$L\frac{d}{dt}\mathbf{i}_{S\alpha\beta} = \mathbf{v}_{S\alpha\beta} - \mathbf{v}_{\alpha\beta} + L\frac{d}{dt}\mathbf{i}_{0\alpha\beta}, \quad (7)$$

where

$$\mathbf{v}_{S\alpha\beta} = \mathbf{v}_{G\alpha\beta} - r_G\mathbf{i}_{S\alpha\beta} - L_G\frac{d}{dt}\mathbf{i}_{S\alpha\beta},$$

and $\mathbf{T} \in \mathbb{R}^{2\times 3}$ is the $\alpha\beta$-transformation matrix (Duesterhoeft et el., 2015). Also as previously denoted, $\mathbf{i}_{S\alpha\beta}$ are the grid currents, $\mathbf{v}_{G\alpha\beta}$ grid voltages, $\mathbf{i}_{0\alpha\beta}$ load currents and $\mathbf{v}_{S\alpha\beta}$ the PCC voltages expressed in $\alpha\beta$-scheme.

2.1.2 Voltage Dynamics

The capacitor voltage dynamics can be represented as

$$C\frac{d}{dt}v_{Cpj} = -\frac{1}{R}v_{Cpj} + u_{pj}i_p, \tag{8}$$

for any particular phase $p \in \{1,2,3\}$ and H-bridge $j \in \{1,\cdots,N\}$. For the convenience of the controller design task, we introduce the following transformation

$$z_{pj} = \frac{v_{Cpj}^2}{2}. \tag{9}$$

Hence, expression (8) becomes

$$C\frac{d}{dt}z_{pj} = -\frac{2}{R}z_{pj} + v_{pj}i_p \tag{10}$$

Furthermore, defining the vectors $\mathbf{z}_p = [z_{p1} \quad \dots \quad z_{pN}]^\intercal \in \mathbb{R}^N$, $\mathbf{v}_p = [v_{p1} \quad \dots \quad v_{pN}]^\intercal \in \mathbb{R}^N$, the previous dynamics result in

$$C\frac{d}{dt}\mathbf{z}_p = -\frac{2}{R}\mathbf{z}_p + \mathbf{v}_p i_p. \tag{11}$$

Also, let

$$\mathbf{A} \triangleq \begin{bmatrix} 1 & 1 & 1 & \dots & 1 \\ 1 & -(N-1) & 1 & \dots & 1 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & 1 & \dots & -(N-1) \end{bmatrix} \in \mathbb{R}^{N\times N}$$

whose $\det(\mathbf{A}) \neq 0$, and $\mathbf{y}_p = [y_{p1} \quad \dots \quad y_{pN}]^\intercal \in \mathbb{R}^N$, the following expression is obtained,

$$\mathbf{y}_p = \mathbf{A}\mathbf{z}_p. \tag{12}$$

So

$$\begin{aligned} C\mathbf{A}\frac{d}{dt}\mathbf{z}_p &= -\frac{2}{R}\mathbf{A}\mathbf{z}_p + \mathbf{A}\mathbf{v}_p i_p \\ C\frac{d}{dt}\mathbf{y}_p &= -\frac{2}{R}\mathbf{y}_p + \boldsymbol{\delta}_p i_p \qquad p \in \{1,2,3\} \end{aligned} \tag{13}$$

where $\boldsymbol{\delta}_p = [\delta_{p1} \quad \cdots \quad \delta_{pN}]^\intercal = \mathbf{A}\mathbf{v}_p \in \mathbb{R}^N$ is a new control input. From (13) and taking into account $p \in \{1,2,3\}$ to the first state in $\mathbf{z}_p$ represents a signal proportional to the cumulative energy of the capacitors in each H-bridge, and the remaining ones correspond to the differences. Thus, the dynamics are analyzed in two sets

$$C\frac{d}{dt}y_{p1} = -\frac{2}{R}y_{p1} + \delta_{p1}i_p, \tag{14}$$

$$C\frac{d}{dt}y_{pj} = -\frac{2}{R}y_{pj} + \delta_{pj}i_p, \quad j \in \{2,\cdots,N\}. \tag{15}$$

As a result, expression (14) presents the dynamics of the sum of the squared capacitor voltages, and (15) models the dynamic behavior of the voltage differences, which is a convenient representation of both the *regulation* and *balance* control objectives to be stated in the upcoming sections.

2.2 ***Control Objectives***

Based on the assumptions detailed in our previous work in (Valdez et al., 2015) and according to the 3-phase CHB-nL converter system generalized model represented in (7), (14) and (15), the performance objectives of the extended controller scheme are defined as follows:

- ***Tracking*** - From (7), a current tracking loop has to be designed to force the grid current $\mathbf{i}_{S\alpha\beta}$ to follow a given reference signal represented by $\mathbf{i}^*_{S\alpha\beta}$. This control objective can be expressed mathematically as, $\mathbf{x}_0 \to \mathbf{i}^*_{S\alpha\beta}$ as $t \to \infty$, with the current reference designed according to $\mathbf{i}^*_{S\alpha\beta} = \dfrac{1}{v^2_{S,RMS}}\mathbf{TP} \bullet \mathbf{v}_S$.

  Notice that $\mathbf{P} = [P_1 \;\; P_2 \;\; P_3]^\intercal$ represents a vector of the active power references, and $\bullet$ the Hadamard product.
- ***Regulation*** - Relying on (14), this control law has to be designed to regulate roughly, the sum of the squared capacitor voltages toward a desired constant reference, that is, $y_{p1} \to \frac{N}{2}V_d^2, p \in \{1,2,3\}$, where V_d is a desired reference for each capacitor voltage v_{Cpj}. This proposal guarantees that enough energy has been stored in every capacitor for the correct fulfillment of the tracking objective.
- ***Balance*** - Dealing with (15), this control law has to be designed to reduce roughly, the sum of the difference of the squared capacitor voltages in an individual phase to zero, that is, $y_{pj} \to 0, \forall p \in \{1,2,3\},\ j \in \{2,3\cdots,N\}$.

3. CONTROLLER DESIGN

In order to fulfill the objectives stated in the previous section, the controller design can be divided into three loops, as explained next.

3.1 ***Current Tracking Loop***

A control input $\mathbf{v}_{\alpha\beta}$ is built based on the energy shaping plus damping injection methodology of the PBC philosophy, from which a copy of a subsystem to be controlled, in this case (7) is made, and then this subsystem is evaluated at the desired reference. After that, the required damping term is added (Ortega et al., 1998), (Escobar et al., 2007), (Sandoval et al., 2012), (Valdez et al., 2013). Therefore, expressing (7) in terms of an error

$$\tilde{\mathbf{i}}_{S\alpha\beta} = \mathbf{i}_{S\alpha\beta} - \mathbf{i}^*_{S\alpha\beta}, \tag{16}$$

yields the following expression

$$L\frac{d}{dt}\tilde{\mathbf{i}}_{S\alpha\beta} = \mathbf{v}_{S\alpha\beta} - \boldsymbol{\delta}_{\alpha\beta} + \underbrace{L\frac{d}{dt}\mathbf{i}_{0\alpha\beta} - L\frac{d}{dt}\mathbf{i}^*_{S\alpha\beta}}_{\phi}, \tag{17}$$

where ϕ represents harmonic disturbances. Based on the structure of (17), the following control signal $\boldsymbol{\delta}_{\alpha\beta}$ is proposed

$$\boldsymbol{\delta}_{\alpha\beta} = k_1\tilde{\mathbf{i}}_{S\alpha\beta} + \mathbf{v}_{S\alpha\beta} + \hat{\phi}\,. \tag{18}$$

The closed-loop system of the subsystem (17) and controller (18) yields the following perturbed linear time-invariant (LTI) system, which is referred to as the error dynamics

$$L\frac{d}{dt}\tilde{\mathbf{i}}_{S\alpha\beta} = -k_1\tilde{\mathbf{i}}_{S\alpha\beta} - \hat{\phi} + \phi, \tag{19}$$

where $k_1 > 0$, is a design parameter used to insert the required damping in order to reinforce stability, and $\hat{\phi}$ to be defined later, is the harmonic compensation term. This type of compensation has been addressed using different schemes, for example the Internal Model principle (Francis and Wonham, 1975). Hence we could either introduce a bank of resonant filters tuned at the harmonic under compensation, or introduce a repetitive scheme (Escobar et al., 2007) and (Castelló and Griñó , 2006). In this work, we choose the following resonant filters

$$\hat{\phi} = \sum_{\ell\in\mathcal{H}} \frac{\gamma_\ell s}{s^2 + 2\zeta\ell\omega_0 s + \ell^2\omega_0^2}\tilde{\mathbf{i}}_{S\alpha\beta}, \tag{20}$$

where $\omega_0 = 2\pi f_0$, ζ is the damping factor, γ_ℓ with $\ell \in \mathcal{H}$ is a positive design parameter representing the gain of the ℓ^{th} harmonic oscillator. Since we are dealing with the 3-phase system, the harmonics set $\mathcal{H}$ is defined as $\{1, 5, 7, 13, \cdots\}$.

3.2 ***Regulation Loop***

The regulation objective is approached by assuming that the current tracking objective has been reached (decoupling assumption) (Valdez et al., 2015), that is, $\mathbf{i}_{S\alpha\beta} = \mathbf{i}^*_{S\alpha\beta}$, $\hat{\phi} = \phi$, which is similar to $\mathbf{i}_S = \mathbf{i}^*_S$. Substituting these conditions in (14) and organizing terms yields the following expression

$$\dot{y}_{p1} = -\frac{2}{R} y_{p1} + g_p v^2_{Sp} + \phi_1, \qquad p \in \{1, 2, 3\} \tag{21}$$

where ϕ_1 is a disturbance signal that contains the higher order harmonics of ϕ, and $g_p \triangleq P_p / v^2_{S,RMS}$, is a variable that represents the apparent conductance observed by the source, which is due to the parallel connection of the load and the active filter, and P_p represents the active power reference in p-phase. Hence, the regulation objective is approached by designing g_p, which is an essential factor for the construction of $\mathbf{i}^*_{S\alpha\beta}$. The structure of this control loop uses a proportional plus integral (PI) scheme to adjust the error signal $\tilde{y}_{pj}$, as follows

$$g_p v^2_{Sp} = \kappa \tilde{y}_{p1} - \xi \int_0^t \tilde{y}_{p1} dt \qquad p \in \{1, 2, 3\}, \tag{22}$$

where κ and ξ are the proportional and integral gains, respectively.

3.3 ***Voltage Balance Loop***

As in Section 3.2, the balance objective is approached by assuming the decoupling condition, that is, $\mathbf{i}_{S\alpha\beta} = \mathbf{i}^*_{S\alpha\beta}$, $\hat{\phi} = \phi$, similarly $\mathbf{i}_S = \mathbf{i}^*_S$. Then taking these conditions in (15) and organizing terms, the following expressions are obtained

$$C\dot{y}_{pj} = -\frac{2}{R} y_{pj} + \frac{\delta_{pj}}{v_{S,RMS}} \left(g_p v^2_{Sp} - v_S i_{0p} \right), j \in \{2, \cdots, N\}. \tag{23}$$

Then control inputs δ_{pj} are designed to force the difference of the squares of the capacitor voltages to zero. It is proposed to build this control loop as

$$\frac{\delta_{pj}}{v_{Sp}} = -\kappa_{pj} y_{pj} - \xi_{pj} \int_0^t y_{pj} dt, \; j \in \{2, \cdots, N\}, \tag{24}$$

where κ_{pj} and ξ_{pj}, are proportional and integral gains of the above mentioned PI control action.

4. NUMERICAL RESULTS

The proposed extended control methodology has been numerically evaluated in a 3-phase SAPF based on a seven-levels CHB (CHB-7L) topology, that is, $N = 3$ H-bridges per phase. The employed parameters during the evaluation stage are: RMS value of the source voltage 127 V_{RMS}, nominal frequency $f_0 = 60$ Hz, inductance of SAPF $L = 4.2$ mH and the capacitances in each H-bridge $C = 2200$ μF. The non-linear load is represented by a full-wave rectifier that includes a smoothing inductor

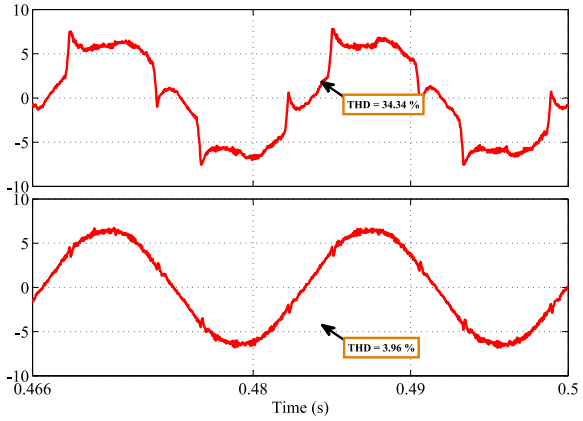

Fig. 2. *Steady state responses of current of phase-1 current: without harmonic compensation* **(top)** *(THD=34.34%); including the harmonic compensation* **(bottom)** *(THD=3.96%).*

of $L_0 = 0.5$ mH, and in order to test the response of the SAPF under load step changes, R_0 is switched during the simulation time between 100 Ω and 50 Ω. The discrete-controller scheme has been implemented in SimuLink/MatLab, with a sampling frequency of $f_s = 55$ kHz.

4.1 ***Steady-State Evaluation***

As mentioned in Section 3.1, the periodic disturbances affect the quality of the source currents i_{Sp}. This effect can be demonstrated in Fig. 2, in which both the current obtained by a conventional controller based on a proportional term to add damping, $\boldsymbol{\delta}_{\alpha\beta} = k_1 \tilde{\mathbf{i}}_{S\alpha\beta} + \mathbf{v}_{S\alpha\beta}$, without harmonic compensation $\hat{\phi}$, and the current that includes the harmonic compensation in phase-1 are illustrated. As expected, the uncompensated current shows a higher harmonic distortion (THD=34.34 %), compared to the compensated one (THD=3.96 %).

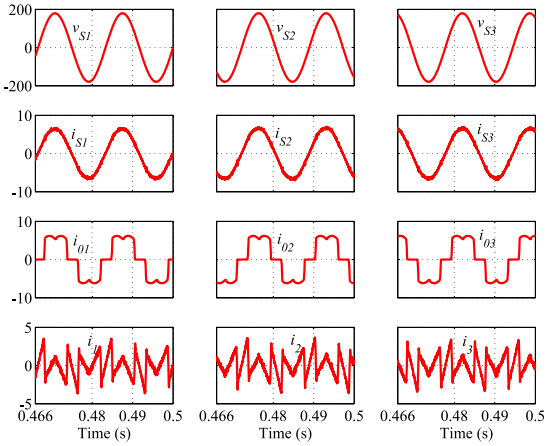

Fig. 3. *Steady-state response of the SAPF under the extended controller solution.* **(Column-wise from left to right)** *phases-1, 2 & 3, and* **(Row-wise from top to bottom)** *source voltages v_{Sp}, compensated currents i_{Sp}, load currents i_{0p} and injected currents i_p.*

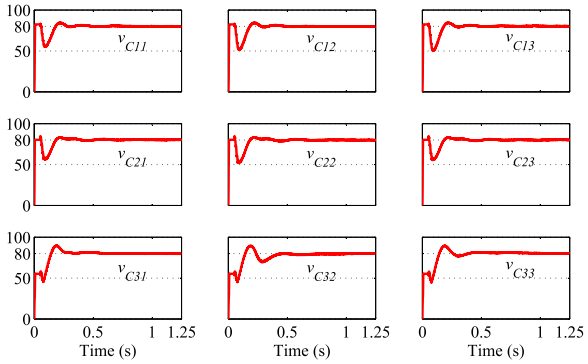

Fig. 4. *Capacitor voltages v_{Cpj},* **(column-wise from left to right)** *phases-1, 2 & 3, and* **(row-wise from top to bottom)** *H-bridges 1, 2 & 3, during the startup of the proposed extended controller.*

Moreover, since the grid currents i_{Sp} are contaminated by the presence of harmonics generated by the NL load, the only way to get these currents to be in-phase with v_{Sp} is to guarantee that $i_{S\alpha\beta}$ follows $i^*_{S\alpha\beta}$. This is possible if the SAPF working under the proposed controller is capable of injecting appropriate currents i_p as shown in Fig. 3. This figure indicates the source voltages v_{Sp}, compensated grid currents i_{Sp}, load currents i_{0p} and the injected currents i_p.

Figure 4 shows the fulfillment of both regulation and balance objectives by indicating the response of the capacitor voltages v_{Cpj}. Notice that, after relatively short transients, all capacitor voltages converge towards the constant reference fixed at $V_d = 80$ V. This condition guaranties that enough energy is stored in the capacitor to make sure that the active filter is capable of injecting the necessary current to cancel the harmonic distortion produced by the NL load.

4.2 ***Load Perturbations Analysis***

This section aims to asses the behavior of the extended controller during the presence of load perturbations. The disturbances are emulated through the introduction of the step changes in the load resistance R_0 (from 50 Ω to 100 Ω, then back to 50 Ω), at time $t = 0.9$ *s* and $t = 1.4$ *s*, respectively. As a result, Fig. 5 indicates the compensated grid currents i_{Sp}, during the above mentioned load change scenario. Observe that a slightly small distortion is introduced during the abrupt changes, which is then minimized by the proposed extended controller. Meanwhile, Figure 6

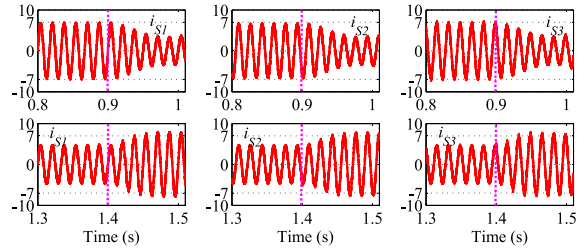

Fig. 5. *Response of compensated currents i_{Sp},* **(column-wise from left to right)** *phases-1, 2 & 3, during step changes in R_0 from 50 Ω to 100 Ω at $t = 0.9$ s* **(top)**, *then back to 50 Ω at $t = 1.4$ s* **(bottom)**.

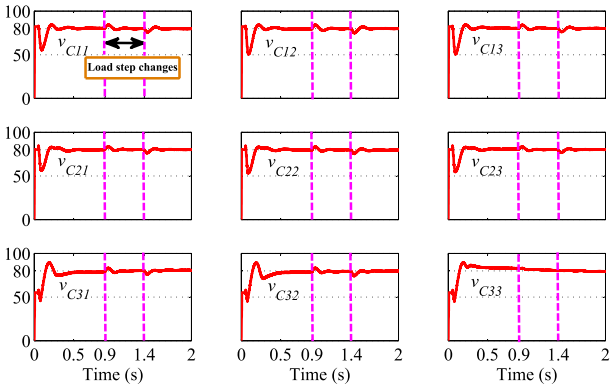

Fig. 6. *Capacitor voltages v_{Cpj} response,* **(column-wise from left to right)** *phases-1, 2 & 3, and* **(row-wise from top to bottom)** *H-bridges 1, 2 & 3, under proposed extended controller during step changes in R_0 from 50 Ω to 100 Ω at $t = 0.9$ s, then back to 50 Ω at $t = 1.4$ s.*

illustrates capacitor voltages v_{Cpj} during step changes in the load resistance, where it can be observed that despite the presence of the rapid changes in the resistance R_0, the proposed controller responded on time and was competent to maintain both *regulation* and *balance* objectives.

4.3 ***Unbalance Condition***

Figure 7 shows the transient response of capacitor voltages v_{Cpj} during the initiation (startup) of the controller under initial unbalance conditions. This figure shows that as soon as the controller is enabled, the voltages in the capacitors converge towards the reference $V_d = 80$ V after a damped transient. Also, Fig. 8 indicates the transitory response when a resistance of 100 Ω is connected to the DC-bus capacitors of the first H-bridges within phases 1 and 2 (v_{C11}, v_{C21}), for a period of time to create an unbalance situation in the system. Observe that when the resistors are connected at $t = 1.5$ *s* and disconnected, a transient occurs almost in all the plotted signals, however,

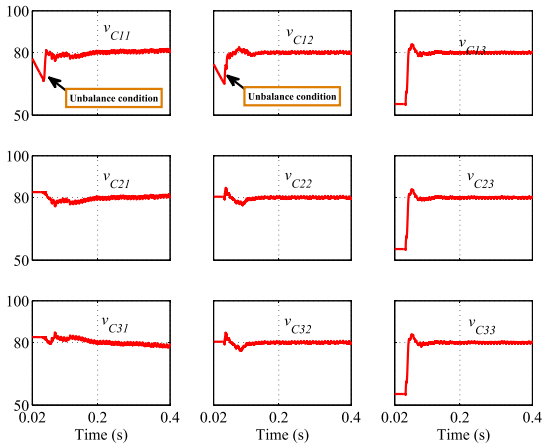

Fig. 7. *Capacitor voltages v_{Cpj} response,* **(column-wise from left to right)** *phases-1, 2 & 3, and* **(row-wise from top to bottom)** *H-bridges 1, 2 & 3, during startup under unbalance initial conditions in the DC-bus capacitors of the first H-bridges within phases 1 and 2.*

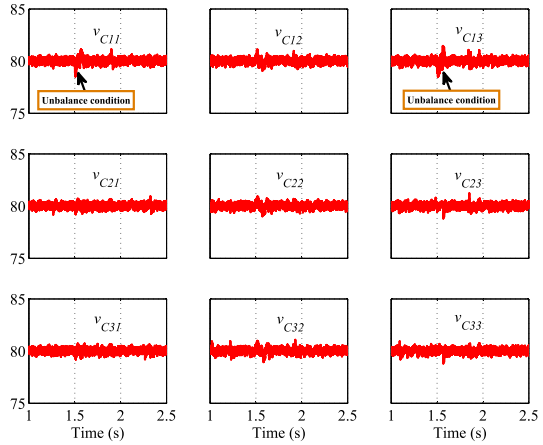

Fig. 8. *Transient responses of capacitor voltages* v_{Cpj}, **(column-wise from left to right)** *phases-1, 2 & 3, and* **(row-wise from top to bottom)** *H-bridges 1, 2 & 3, under unbalance conditions triggered during the steady state, at* $t = 1.5\ s$.

after a short period of time, the capacitor voltages v_{Cpj} go back to their reference value $V_d = 80$ V.

CONCLUDING REMARKS

This paper presented the generalized modeling and controller design of 3-phase CHB-nL converters used as a SAPFs. Based on the generalized model, a closed-loop controller was proposed to compensate harmonic distortions and reactive power caused by NL loads, simultaneously maintaining the balance condition in the capacitors voltages. The controller comprised three generalized loops, namely, current tracking loop, voltage regulation loop and voltage balance loop. The current tracking loop guaranteed tracking of the line current, while voltage regulation and balance loops guaranteed regulation and balance of the involved capacitor voltages toward constant references. The new generalized state variables were suggested in such a way that the extended controller can be applicable in any arbitrary number of H-bridges. Simulation results using a CHB-7L converter with $N = 3$ bridges were presented to assess the performance of the proposed controller. The behavior of the proposed controller due to the step changes in load side and unbalance conditions was also tested.

As a future work, the experimental implementation of the 3-phase CHB-7L converter will be pursued under different operating scenarios. Where from, the DS1103 PPC Controller Board will be used for the implementation of the control laws in (18) (22) and (24), since it posses libraries for directly communication with SimuLink, which avoids the task of writing code in C++ or other low/middle level programming languages.

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