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Comparative Performance Evaluation of dSPACE based PLL Algorithms for Grid-connected Single-Phase Converters

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Abstract: To obtain optimum performance from renewable sources interconnected to the AC electrical network, it is necessary to have adequate monitoring and synchronization with the AC network. In equipment based on power electronics, the grid synchronization has been achieved by Phase Locked Loops (PLL) algorithms, in order to ensure stable operation. The aim of this paper is to compare the performance of three PLL algorithms under different disturbances: second-order PLL, Fourier-based PLL, and Inverse Park Transformation (IPT) PLL. This study is carried out using a dSPACE platform where PLL models are implemented in the Simulink interface. The parameters considered in the comparison are the settling time, the performance before a smooth frequency variation and interrupt disable. These comparisons show that PLL IPT has the worst performance before an input interruption occurs. PLL based on second order generalized integrator (SOGI) has the shortest settling time and the PLL Fourier performance is quite similar to the former in settling time and when a smooth frequency variation is applied. These results provide a guide to choose the best PLL structure for any applications related to interconnected single-phase power converters , and considerations to be taken into account.

Keywords: Phase Locked Loop (PLL), single-phase, phase estimation, synchronization, PLL SOGI, PLL Fourier-based, Inverse Park Transformation PLL.

1. INTRODUCTION

Nowadays, there is a wide proliferation around the world of distributed power generation systems based on alternative sources, such as photovoltaic, fuel cells and wind energy. The development of these systems helps to cover the increase in energy demand, with a reduced effect of harmful emissions and pollution. Although they are feasible, renewable energies are uncertain and often unavailable at the time of demand; for these reasons, controllability of these systems is more challenging [Blaabjerg et al. (2004)]. To obtain an optimal performance from renewable sources interconnected to the AC mains, it is necessary to have adequate monitoring and synchronization to the network, due to the fact that it is affected by multiple eventualities such as the continuous connection and disconnection of loads, disturbances and resonances. These disturbances are due to the normal operation of the loads, the distorted currents (harmonics) flowing through the lines, the failures due to lightning and the malfunctioning of the electrical equipment [Han et al. (2016)]. In this sense, the estimation of amplitude, frequency, and grid voltage phase-angle has become a fundamental issue in this kind of applications [Ciobotaru et al. (2006)].

The grid synchronization has been achieved by Phase Locked Loops (PLL) algorithms in power electronics based equipment such as dynamic voltages restorers, uninterruptible power system, among others, with the purpose of ensure stable operation of grid-connected [Ciobotaru et al. (2006)], [Silva et al. (2004)], [Setiawan et al. (2016)], [Golestan et al. (2017)]. However, to assure a suitable performance on these converters interfacing to the ac-mains requires a PLL algorithm capable of maintaining grid utility synchronization during voltage sags and swells, presence of harmonics, phase and frequency jumps and noise. Therefore, several PLL structures have been reported in the literature searching for a reliable performance [Han et al. (2016)], [Fang et al. (2010)], [Karimi-Ghartemani and Iravani (2004)], [Ciobotaru et al.

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(2008)].
In recent years, some papers in the literature have studied with specific PLL topologies trying to find useful information by comparatives studies. The main purpose is to give a general sight about PLL performance parameters to choose the best one according to the application. For example, [Silva et al. (2004)] presents a comparative study among three PLL algorithms, namely, Inverse Park-Based PLL, discussed in [Timbus et al. (2005)], Hilbert Transformer-Based PLL [Saitou et al. (2003)] and Transport delay PLL. The objective is to evaluate their behaviour under distorted utility conditions like angle and amplitude deviation, and experimental implementation is reported. Also, a very extensive survey is presented in [Han et al. (2016)] where eight PLL algorithms are evaluated. In this case disturbances like voltage sags, frequency overshoot and direct current offset were evaluated. Besides, the settling time is measured. The pair of paper mentioned before show that PLL performance evaluation during amplitude and frequency disturbances has great importance and it is a well parameter to discriminate among a PLL and another.

As an important remark, the aforementioned studies only consider Orthogonal-Signal Generators-Based that is the most common way to generate an error signal between the reference and the PLL response. However, there exists papers which use others methods and structures to form a PLL loop and, how is shown in this work, have similar performance parameters Orthogonal-Signal Generators-Based PLL, for example PLL SOGI. Additionally, in the literature the frequency variations, as a PLL disturbance, has been tested but all of them only consider instantaneous variations and a smooth variations are not considered. In this sense, the main aim of this paper is to complement the comparative study proposing a set of PLL whose structures differ taking in account a Orthogonal-Signal Generators-Based structure, a frequency domain structure and an Park Transformation based structure. Also, an evaluation with smooth frequency variations are proposed to show the PLL performance is affected under this disturbance.

This paper presents the evaluations of the performances of PLL based on SOGI introduced in [Ciobotaru et al. (2006)], a Fourier-Based PLL reported in [Santos et al. (2010)] and Inverse Park-Based PLL [Zheng Wang et al. (2012)] on a dSPACE device, which is a software and hardware real-time control platform based on MATLAB/Simulink, which is widely used in robotics, aerospace, engines and industrial control. dSPACE device was selected because it has the advantage that not only models can be described using Simulink interface, also the disturbances can be generated due the analogic and digital interface that it has. Besides, it has been used to make comparisons due the easy implementation in practice [Han et al. (2016)].

The comparison consists on determining the settling time before the algorithm begins to compute, a smooth frequency disturbances and a disabling of input reference.

The paper is organized as follows: in Section 2 a brief description of PLL structure is given and the PLL topologies compared are presented. Section 3 describes each one of tests implemented under different disturbances. In Section 4 the experimental results are shown. Finally, the conclusions of this work are given in Section 5.

2. PLL OVERVIEW

Grid synchronization of single-phase grid-connected converters lies in the accurate detection of the attributes of the grid voltage, in order to tune an internal oscillator of the power converter controller to the oscillatory dynamics imposed by the grid [Teodorescu et al. (2010)]. The grid synchronization techniques can be classified in two main groups, namely the frequency-domain and the time-domain detection methods; the former set is usually based on some discrete implementations of the Fourier analysis and the latter is based on adaptive loop that enables an internal oscillator to track the component of interest of the input signal. The most extended method is called PLL, which is a closed-loop system with an internal oscillator controlled to keep the time of the external reference.

2.1 General PLL Structure

A PLL is composed by three primary sections: phase detector, loop filter, and a voltage-controlled oscillator as shown in Fig. 1. The phase detector generates an output signal proportional to the phase difference between the input signal v, and the signal generated by the internal oscillator of the PLL, v'. Depending on the type of phase detector, high-frequency AC components appears together with the DC phase-angle difference signal [Han et al. (2016)].

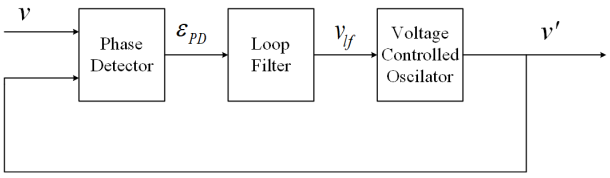

Fig. 1. Basic structure of a PLL.

The loop filter presents low-pass filtering characteristics to attenuate the high-frequency AC components from the phase detector output. Regularly, it consists of a first-order low-pass filter or a PI controller. The voltage-controlled oscillator generates at its output an AC signal whose frequency is shifted with respect to a given central frequency ω_c, as a function of the input voltage provided by the loop filter. In [Teodorescu et al. (2010)] PLL model description can be found. Using this model, it is

possible to get equations which describe the performance parameters. They are related with the PI parameters and are given by:

$$K_p = 2\xi\omega_n = \frac{9.2}{t_s}, \tag{1}$$

$$T_i = \frac{2\xi}{\omega_n} = \frac{t_s\xi^2}{2.3}, \tag{2}$$

where ω_n is the natural frequency, ξ is the PLL damping, t_s is the settling time, K_p is the PI proportional gain and T_i the integral time. Hence, by proposing the parameters ω_n, ξ or t_s, K_p and T_i can be founded.

2.2 PLL algorithms

Once the PLL structure has been presented, consider now the Fig. 2 where a PLL diagram is shown. This diagram presents the elements which were mentioned above, namely, Phase detector (1), Loop filter (2), and Voltage controlled oscillator (3), (4). Also, additional elements are displayed as the output multiplier, the integrator to obtain the angular frequency and in order to set the central frequency of PLL.

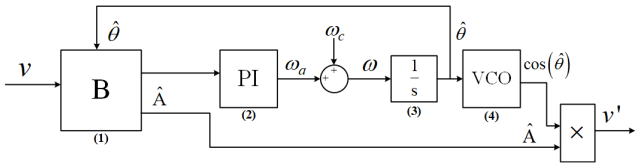

Fig. 2. General structure of a PLL.

In the Fig. 2 where Â is the amplitude estimation, ω is the angular frequency and θ is the angle estimation, is observed that the main difference between a specific PLL and another lies the structure of the block B, which can be an orthogonal signal generator [Ciobotaru et al. (2006)], [Golestan et al. (2017)]; the main idea is to emulate a three-phase system with the Park Transformation because this approach does not generate steady-state oscillatory terms in the model, which allows the PLL bandwidth to increase, unlike using a multiplier in the phase detector [Teodorescu et al. (2010)]. Other kind of elements can estimate the angular frequency error and the amplitude Santos et al. (2010). In this sense, three different PLL topologies were selected to study, namely, PLL SOGI introduced in [Ciobotaru et al. (2006)], a Fourier-based PLL proposed in [Santos et al. (2010)], and from now it will be refer as PLL Fourier, and Inverse Park-Based PLL refers as PLL IPT (Inverse Park Transformation) [Zheng Wang et al. (2012)]. They were selected for two principal reasons: the first was that all of them have different structures for estimating the angular frequency error, PLL SOGI uses an integrator and dq transformation, PLL Fourier PLL uses the Fourier's series expressions and PLL IPT uses Park transformations and Inverse Park transformation loop. The second one is that SOGI and IPT PLLs are well-known in the literature, even in comparative studies, then this work complements the previous one. Additionally, PLL Fourier proposes an a different approach to the other ones which can have the same performance than the others do. They are described below.

2.2.1 PLL SOGI.

PLL SOGI was introduced in [Ciobotaru et al. (2006)] and presents a method to create an orthogonal signal based on second order generalized integrator (SOGI). The general structure of PLL SOGI is shown in Fig. 3, where the complete structure is shown in Fig. 3 **(a)** and SOGI block in Fig. 3 **(b)**. "the first one is a low-pass filter and the second one a numeric integrator in order to get a signal qv with a phase shift of 90° with respect v. The

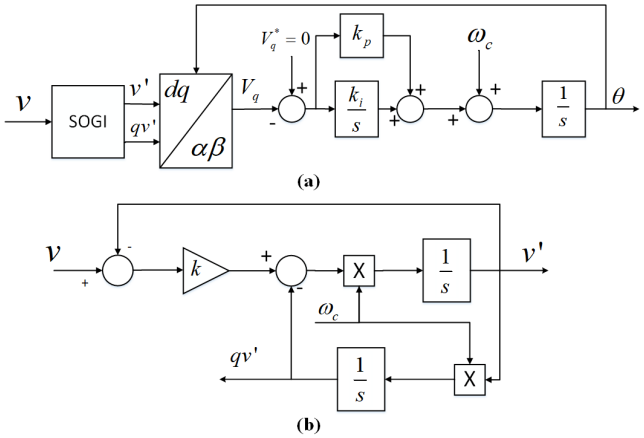

Fig. 3. General structure of a PLL SOGI.

SOGI structure can be described by two transfer function $H_d(s)$, the low-pass filter, in terms of input signal v and output qv' which given by:

$$H_d(s) = \frac{v'}{v}(s) = \frac{k\omega_s s}{s^2 + k\omega_s s + \omega_s^2}, \tag{3}$$

and the integrator $H_q(s)$ defined by:

$$H_q(s) = \frac{qv'}{v}(s) = \frac{k\omega_s^2}{s^2 + k\omega_s^2 s + \omega_s^2}, \tag{4}$$

where k affects the bandwidth of the closed-loop system and ω_s represents the resonance frequency of the SOGI.

2.2.2 PLL Fourier.

The PLL Fourier is presented in [Santos et al. (2010)], it applies the principle of Fourier series to estimate the angular frequency error and as the same way the amplitude estimation. The multiplication of the input signal by sine wave is performed by the PD. In fact, the structure is the one that is shown in Fig. 2, but the difference lies on the block B and dq transformation which are replaced by the matrix

$$Q = \begin{pmatrix} -\sin(\theta) & \dfrac{\sin 2\theta}{2} \\ \cos(\theta) & \dfrac{-\cos 2\theta}{2} \end{pmatrix}, \tag{5}$$

which is multiplied by the vector $\left[\, v \;\; \hat{\mathrm{A}} \,\right]^T$.

2.2.3 PLL IPT.

The PLL IPT consists of an algorithm which takes advantage of the Park Transformation. Fig. 4 shows a schematic diagram of IPT PLL. As it can be seen, single phase voltage V_β and an internally generated signal V_α are used as inputs to a Park transformation block ($\alpha\beta$-dq). The d component is used in a control loop to obtain phase and frequency information of input signal. On the other hand, V_β is obtained through the use of an inverse Park transformation, where the inputs are the d and q outputs of Park transformation. Additionally, two low-pass filters are added to minimize the oscillations during the estimation and they can be tuned by ρ.

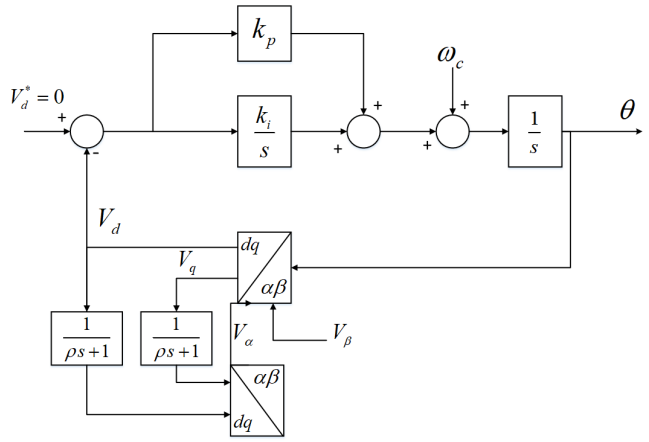

Fig. 4. General structure of a PLL IPT.

3. BENCHMARK DESCRIPTION

The main aim of this paper is to make a comparison among three PLL algorithms described below to evaluate their performance during several input disturbances. In this sense, three experiments are proposed. The first one consists of determining the settling time when the algorithm starts; the second one consists of measuring the settling time after a smooth frequency variation, and the last one consists of determining settling time and evaluate whether the synchronization is maintained or not, these experiments are described below:

(1) **Settling time experiment.**
Consists of determining the time until relative error between the input and PLL output reaches 10% or less after algorithm starts.
(2) **Smooth frequency variation experiment.**
Consists of determining the time until relative error between the input and PLL output reaches 10% or less after a smooth frequency variation of 0.1 Hz during 1 second.
(3) **Input Disable experiment.**
Consists of determining the settling time before the input reference is disabled during 0.1s and verify whether the PLL algorithm is able to remain synchronized.

The experiments were performed with the following considerations:

(1) PLL algorithms were performed in a dSPACE 1103 device using MATLAB/Simulink interface.
(2) The sample frequency used in the experiments is $f_s = 16.384$ kHz with a period of T_s=61.03 μs.
(3) Numerical integration fourth order Runge-Kutta method is used.
(4) The input reference signal in experiments is generated using dSPACE 1103 device.
(5) The reference signal amplitude is 1 V in all experiments.
(6) The reference signal frequency is 60 Hz.
(7) The PLL algorithms were designed proposing settling time $t_s = 0.01$ s and damping factor $\xi = 1$.

The sampling frequency f_s was selected taking into account the fact of dSPACE's manual recommends the use of power of 2 numbers in constants definitions, signal frequencies and the step time values in order to reduce numerical problems due the precision in 32 bits floating point format. Using sample time that can be represented in the binary format can achieve better simulation accuracy in Simulink models. Therefore, $T_s = 2^{-14}$ s was chosen which implies $f_s = 16.384$ kHz .

Furthermore, the experiments were made according with the diagram in the Fig.5. The reference signal is generated on dSPACE device and then is converted into an analog signal by a DAC port, in order that it can be read by dSPACE ADC. Additionally, a second DAC port is used to measure the PLL output.

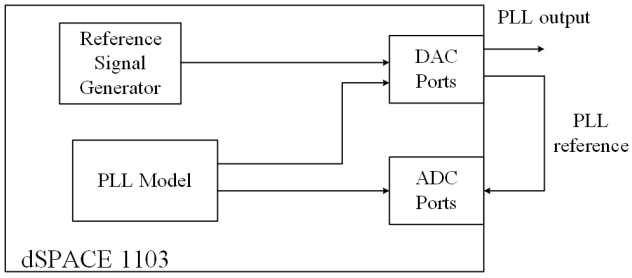

Fig. 5. Scheme of the PLL structure on dSPACE.

4. RESULTS

The results of the experiments mentioned in section 3 are presented in this section. Each measurement shows four signals. Ch 1 is the relative error between the input and the output PLL signal, Ch 2 displays the PLL input, Ch 3 shows a synchronization signal that depends on the experiment and Ch 4 shows the PLL output.

4.1 Settling time experiment

In order to measure the settling time, a synchronization signal is generated by dSPACE, shown in Ch 3 in Fig. 6, which is a logic signal that starts in 0 after the algorithm begins and then it is set to 1 when PLL starts to operate. In Fig. 6 (a) the experiment result for PLL SOGI is presented which presents a settling time of 116 ms. Fig. 6 (b) the results from PLL Fourier have a settling time of 240 ms, and finally Fig.6 (c) shows the results obtained for PLL IPT with a settling time of 260 ms. Notice that, when the time is short it is possible to assure that the reference generated is suitable when the algorithms begins. In other words, during start sequence, all algorithms that depend on the PLL have to wait until the error has an appropriate value.

4.2 Smooth frequency variation experiment

In the experiment 2 a synchronization signal is generated by dSPACE to show when the disturbance starts, that is shown in Ch 3. The experiment results for PLL SOGI is presented in Fig. 7 (a) with a time of 112 ms. Then, in Fig. 7 (b) the results from PLL Fourier with 102 ms and finally in Fig. 7 (c) shows the results obtained for PLL IPT with 260 ms. For this experiment, to ensure the minimum settling time after the disturbance guarantees the stability of the PLL reference and the stages which uses PLL output (phase, amplitude).

4.3 Input disable experiment

At the experiment 3 the PLL response after an input interruption is presented. In order to induce this disturbance, a square signal is generated with a period of 0.2 s, this is multiplied by the input signal and before the settling time is determined. The square signal is shown in the Ch 3 Fig. 8. As it can be seen, the PLL SOGI has a time of 50.4 ms (Fig. 8 (a)), the Fourier PLL presents a time of 67 ms (Fig. 8 (b)) and the last one, IPT PLL is not synchronized again then it is impossible to get a settling time (Fig. 8 (c)). This experiment is critical in isolated grids because they might stop working adequately without a stable reference, then having a short settling time ensure a suitable performance after reconnection scenarios.

4.4 Discussion of results

After three experiments it is possible to argue some premises about it. In the first one, settling time experiment, all of PLLs present steady state oscillations at error response, which does not exceed the 100% and during the first three grid cycles that is associated to the time response of the elements that generates the angular frequency error. The PLL algorithm based on SOGI has the shortest settling time among the three topologies due tow possibilities, the first one is the dynamic simplicity and the second one the PLL SOGI estimation is based only in a mathematical operator as the PLL Fourier unlike the IPT has more stages and two filters. Additionally, as is shown in Fig. 6, PLL SOGI presents an underdamped response which must take in account when this algorithm is selected due the error is going to be bigger in the transitory state than the others. In case of experiment 2, as observed in the results the PLL tracking error presents oscillations while the frequency variation occurs and stop when it is fixed again. As is mentioned, in the first experiment all the three algorithms have more than 0.1 s which is relevant information because in any application it is necessary to consider this time at turn on time to guarantee a suitable performance. Then, in experiment 2 the PLL synchronization is not ensured after smooth variations for three cases. Moreover, in gradual changes in frequency PLL does not guarantee a suitable performance only when the frequency is varying. Finally, in experiment 3 PLL SOGI has the shortest settling time after interruption than the others. In case of PLL based on Fourier, it has the same response as the previous PLL but is not synchronized before the interruption in all the experiments then is not possible to assure guarantee the monitoring and the suitable performance under this disturbance. The last one, PLL IPT, can not be synchronized before an interruption, during a set of experiments this algorithm never track the reference with the same disable used with the others PLL. This experiment shows that PLL IPT may not be suitable when the utility is disconnected. The Table 1 summarizes all the results.

Table 1. Results of Experiments

Experiment	PLL SOGI	PLL Fourier	PLL IPT
Settling Time	116 ms	240 ms	260 ms
Frequency variation	112 ms	102 ms	260 ms
Input disable	50.4 ms	67 ms	-

5. CONCLUSION

This paper made a comparison of PLL SOGI, PLL Fourier and PLL IPT through three experiments. PLL topologies were tested under start conditions, smooth frequency variations and input disable. After first experiment, it is possible to conclude that IPT has the biggest settling time and is preferred use PLL SOGI or PLL Fourier when quick begins are required. The second experiment shows that three PLL algorithms are affected by smooth frequency variations, the oscillations during the disturbance can comprise the proper performance and a wide study about this is required. In weak grids such as micro grids this is an important issue, therefore determine if the possible disturbance that could appear in them are inside the range where PLL starts to be unsuitable. The last experiment, which tests the settling time after a interruption, yields to have useful information, especially when the applications is a micro grid or isolated grids. Disconnection and reconnection are possible phenomena in these kind of grid, then not only the settling time is very important but also the certainty of resynchronization. In this sense, PLL IPT has the worst performances because

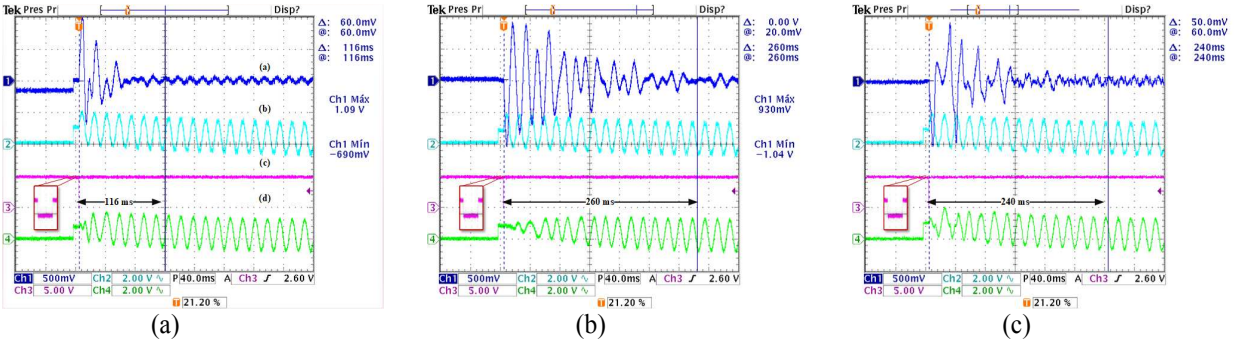

Fig. 6. Time settling measure of: (a) PLL SOGI, (b) PLL Fourier and (c) PLL IPT.

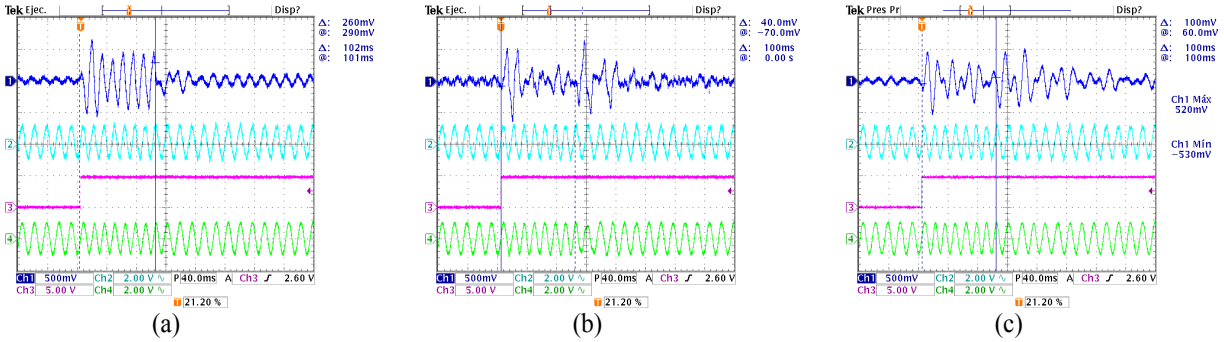

Fig. 7. Smooth frequency variation of: (a) PLL SOGI, (b) PLL Fourier and (c) PLL IPT.

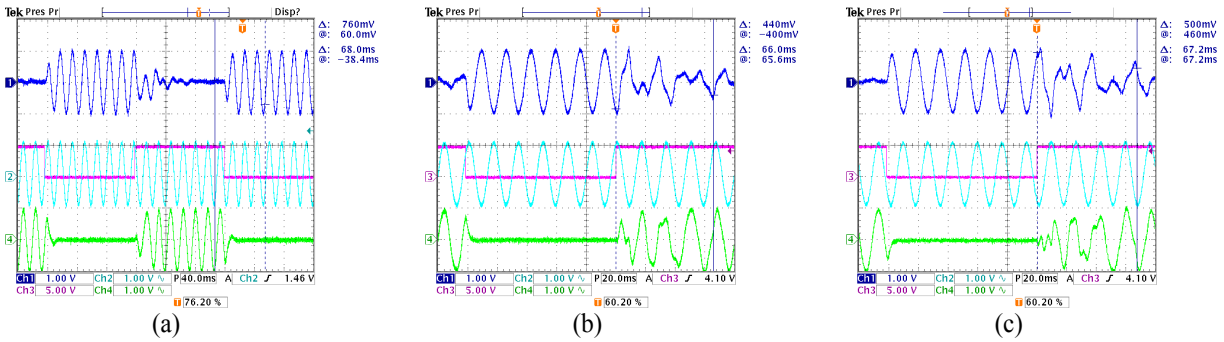

Fig. 8. Time settling after input disable of: (a) PLL SOGI, (b) PLL Fourier and (c) PLL IPT.

of the difficulty to attain the synchronization after the interruptions. Although PLL Fourier get reconnection, it is not sure in all tests. Therefore, a set of experiments have to be made in order to get the maximum and minimum frequency of this interruptions. According to the application is necessary consider all of this constraints when choosing a PLL algorithm. Ongoing work is evaluating the same topologies in other different digital systems like DSP or FPGA and determining whether this performances parameter can be improved.

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