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Circuit implementation and optimisation for current-mode control of DC-DC converters using the lead-lag control technique

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Abstract: In this paper, we present a proposed toolbox designed to calculate the tuning parameters of the current-mode lead-lag phase controller of a boost converter. This toolbox uses user-supplied specifications, such as electronic components, operating values, and step response parameters. Unlike heuristic or numerical optimization techniques, the tuning methodology offers a unique solution for tuning the controller parameters, which is simple to automate. In addition, the toolbox provides simulations and reports on controller tuning parameters. It also presents graphs of the step response, Bode diagram, and control signal. This toolbox stands out due to its validation through implementation on an analog design development board for didactic purposes. In this way, it proves to be a valuable tool for teaching and learning in the field of power electronics and classical control systems.

Keywords: Boost DC-DC converter, Phase lead-lag controller, Toolbox lead-lag Control, App Designer Matlab.

1. INTRODUCTION

Power electronics has benefited from the use of interactive tools such as the interface presented in this article (lead-lag control) and other Matlab toolkits such as SiSOtool and PIDtuning. The lead-lag control tool allows specifying up to three control parameters and observing their effects in the time and frequency domain, facilitating the optimized and efficient exploration of DC-DC power converters.

Furthermore, it is known that in DC-DC power converters, there is an energy storage phase and an energy release phase. During the switch-on time, the inductor stores energy. When the switch is opened, the stored energy is transferred to the capacitor to power the load. There are classic and modern control strategies to control these converters based on the change of the duty cycle. The two main control modes are: voltage mode (one voltage control loop) and current mode (two control loops, one for internal current and one for external voltage).

In this context, in Table 1 the Lead-Lag control tuning strategy proposed by Muñiz-Montero et al. (2016) stands out as an advanced and efficient methodology for tuning its control parameters. Compared to other tuning methods mentioned in the state of the art, such as PI and PID controllers, and sliding mode control, the Lead-Lag strategy offers significant advantages in terms of robustness and system stability. While traditional methods can present difficulties in parameter tuning and unwanted effects such as chattering, Lead-Lag tuning provides an optimized and efficient alternative for the control of DC-DC power converters.

In summary, the design of Boost DC-DC converters with current-mode control using algebraically tuned Lead-Lag controllers is addressed and incorporated into a MATLAB

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AppDesigner tool that automates the design as well as the implementation of an educational analog prototype.

2. THEORETICAL FOUNDATION

2.1 DC-DC Boost Converter

The Boost type DC-DC converter shown in Fig. 1, is a type of switching power supply that has the ability to obtain at its output $V_o(s)$ a higher DC voltage than at its input $V_{in}(s)$. The operation of the Boost converter is based on two different states depending on the state of switch S_1 and S_2:

- Conduction State (Switch S_1 Closed) : In this state, the inductor L stores energy from the source while the load is supplied by the capacitor C.
- No Conduction State (Switch S_2 Open): When the switch is opened for S_2, all the energy stored in coil L is discharged into capacitor C, which now stores the energy generated for later use, as if it were a voltage source at $V_o(s)$, to power the electrical loads.

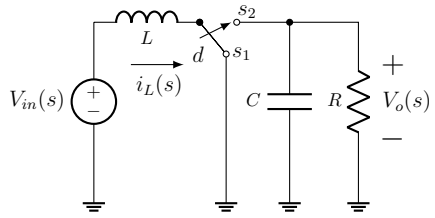


Fig. 1. Boost type DC-DC converter.

It is important to mention that the boost converter has an output voltage $V_o(s)$ higher than the source voltage $V_{in}(s)$, but the output current is lower than the input current $i_L(s)$. In addition, filters constructed with inductors and capacitors are often added to improve performance.

The Fig. 2 shows the block diagram and the electrical schematic of the control of the DC-DC Boost converter. In this circuit the output voltage $V_o(s)$ is regulated to a constant value determined by a reference $U(s)$ and amplified with respect to the input voltage $V_{in}(s)$ by modifying the switching cycle $d(s)$ which is driven by driven by the power transistor M_D, obtaining a gain between the output and input ratio shown in:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{1}{1-D} \tag{1}$$

From the gain ratio of the boost converter and by performing a small signal analysis, the corresponding transfer functions in continuous conduction mode are obtained, which are as follows:

$$G_{id}(s) = \frac{i_L(s)}{d(s)} = \frac{V_o Cs + \frac{V_o}{R}(2-D)}{LCs^2 + \frac{L}{R}s + (1-D)^2} \tag{2}$$

$$G_{voiL}(s) = \frac{V_o(s)}{i_L(s)} = \frac{R}{RCs+1} \tag{3}$$

where $G_{id}(s)$ is the transfer function for the control of the inductor current $i_L(s)$ with respect to the duty cycle $d(s)$ and $G_{voiL}(s)$ is the outer loop transfer function for the control of the output voltage $V_o(s)$ with respect to the controlled inductor current $i_L(s)$. It is worth mentioning that the inner loop control $G_{id}(s)$ has to be faster than the outer loop control $G_{voiL}(s)$, for optimal control of the output voltage.

2.2 Cascade control of the DC-DC Boost converter

The $G_{cv}(s)$ and $G_{ci}(s)$ controllers are incorporated so that $V_o(s)$ and $i_L(s)$ satisfy the scaling response specifications, such as: percentage overshoot (M_p), steady state error (e_{ss}) and settling time at 2% (t_s). The output of $G_{ci}(s)$ is pulse width modulated by the PWM block to obtain $d(s)$. This modifies the duty cycle so that $V_o(s)$ is regulated to the voltage gain given by (1). In this job the boost converter will amplify and regulate a nominal voltage of 46V. The output power will be 17.6W.

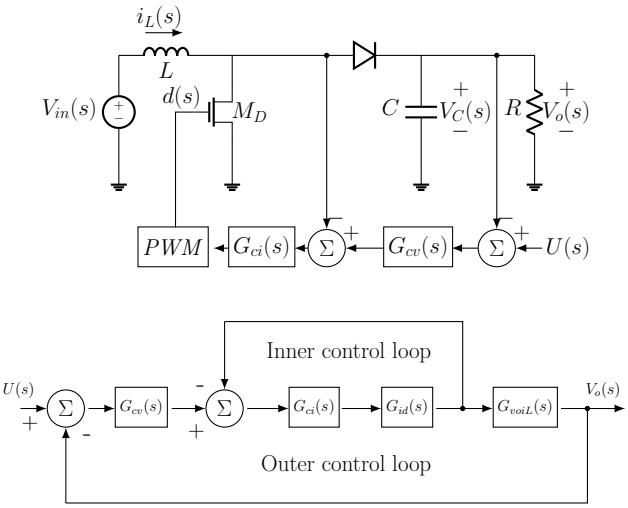


Fig. 2. Cascade control of the DC-DC converter and its block diagram.

2.3 Step response of second order systems

The step response of a second-order underdamped canonical system is characterised by several parameters that describe its transient behaviour (Nise, 2011). These parameters can be calculated from the damping factor ξ the natural frequency ω_n, and the system gain K given these parameters, the following relationships are obtained:

Damping Factor (ξ): This parameter describes the amount of damping in the system. It can be calculated from the maximum overshoot (M_p) using eq. :

$$\xi = \left| -\ln\left(\frac{M_p}{100}\right)\left[\pi^2 + \ln^2\left(\frac{M_p}{100}\right)\right]^{-0.5} \right| \tag{4}$$

Phase Margin (MF): The difference between the phase of the system response and -180° at the gain crossover frequency. It can be calculated from the damping factor (ξ) using:

Table 1. Characteristics of different control strategies for DC-DC converters

Reference	Controller	Parameters	Converter	Advantages	Disadvantages
Anil et al. (2013)	*PI* Controller	Voltage	Buck-Boost	It improves steady-state error, decreases system bandwidth and filters out high-frequency noise.	Ziegler-Nichols tuning rules suggest that improper Ki calculation can lead to instability from pole shifting rightward.
Nagarajan et al. (2016)	*PI* Controller	Voltage	Boost	Optimize transient response and minimize overshoot with Kp, and reduce steady-state error with Ki.	Relative stability is affected by increasing transient response overshoot and oscillations.
Shabrina et al. (2017)	*PID* Controller	Voltage	Boost	Add a low-pass filter to the PID controller's derivative to filter high-frequency noise.	Tuning method based on Ziegler-Nichols and MPC (Model Predictive Controller).
Dinniyah et al. (2017)	*PID* Controller	Voltage	Buck-Boost	The proportional optimizes the process, the integral corrects the proportional constant's error, and the derivative adjusts previous defects.	Tuning uses trial and error techniques.
Utkin (2013)	Sliding Mode Control	Current	Boost	Invariant to perturbations introduced into the system.	Complex sliding surface design and stability criteria.
Xiao et al. (2017)	Sliding Mode Control	Current	Boost	Good convergence rate on the sliding surface.	High frequency switching increases the current ripple.

$$MF(\xi) = \arctan\left(2\xi\left[-2\xi^2+\sqrt{4\xi^4+1}\right]^{-0.5}\right) \quad (5)$$

Bandwidth (ω_{BW}): The frequency at which the magnitude of the system response falls $3dB$ below the low-frequency magnitude. It can be calculated from the damping factor (ξ) and the settling time (t_s) using eq. :

$$\omega_{BW} = \frac{4}{\xi t_s}\sqrt{(1-2\xi^2)+\sqrt{4\xi^4-4\xi^2+2}} \quad (6)$$

Steady State Error (e_{ss}): The difference between the input value and the output value when the system has reached steady state. It can be calculated from the gain margin (M) using:

$$e_{ss} = \frac{100\%}{1+10^{\frac{M}{20}}}, K = 10^{\frac{M}{20}} = \frac{100}{e_{ss}} - 1 \quad (7)$$

2.4 Phase lead-lag controller

In 2003, Wang proposed the following analytical method for lead-lag control tuning Wang (2003). Consider K, M decibels and p radians ($-\pi/2 \leq p \leq \pi/2$) as the direct current gain, magnitude and phase to be provided by the controller at the frequency $\omega=\omega_c$ to obtain the desired e_{ss}, M_p and t_s. This goal is achieved with the lead-lag controller.

$$C(s) = K\left(\frac{1+\alpha\tau s}{1+\tau s}\right) \quad (8)$$

if and only if

$$c > \sqrt{1+\delta^2}, \quad \text{with } 0<p\leq\pi/2 \text{ (lead phase)} \quad (9)$$

$$c < \frac{1}{\sqrt{1+\delta^2}}, \quad \text{with } -\pi/2\leq p<0 \text{ (lag phase)} \quad (10)$$

where $c=10^{M/20}$ and $\delta=\tan(p)$. If (9) or (10) are satisfied, then the parameters α and τ are calculated by

$$\alpha = \frac{c(c\sqrt{1+\delta^2}-1)}{c-\sqrt{1+\delta^2}}, \qquad \tau = \frac{c-\sqrt{1+\delta^2}}{c\delta\omega_c} \quad (11)$$

2.5 Design of lead-lag controllers

In 2016 Muñiz proposes design of $G_{ci}(s)$ and $G_{cv}(s)$ as lead-lag controllers Muñiz-Montero et al. (2016). The main advantage is to obtain them uniquely and exactly by algebraic methods.

$$G_{ci}(s) = K_{int}\left(\frac{1+\alpha_i\tau_i s}{1+\tau_i s}\right)$$
$$G_{cv}(s) = K_{ext}\left(\frac{1+\alpha_e\tau_e s}{1+\tau_e s}\right) \quad (12)$$

(1) Set specifications for e_{ss}, M_p and t_s for the inner and outer loops.
(2) For each loop, with (4) and (5) calculate ξ and MF.
(3) For each loop, with (6) calculate ω_{BW} from t_s and ξ.
(4) For $G_{ci}(s)$, calculate with (7) the gain K_n needed to satisfy e_{ss}. Subsequently, calculate $K_{int}=K_n/G_{id}(0)$. For $G_{cv}(s)$, calculate with (7) the K_n needed to satisfy e_{ss}. Subsequently, calculate $K_{ext}=K_n/K_{LI}(0)$, where:

$$K_{LI}(s) = G_{voiL}(s)\left[\frac{Gci(s)Gid(s)}{1+Gci(s)Gid(s)}\right] \quad (13)$$

(5) For $G_{ci}(s)$ and $G_{cv}(s)$ plot the Bode diagrams of $K_{int}\cdot G_{id}(s)$ and $K_{ext}\cdot K_{LI}(s)$. Then, for each of these responses, determine the magnitude $-M$ in decibels and the phase F in radians at the frequency ω_{BW}.
(6) Calculate for each loop $p=0.5\pi-MF-F$, $\delta=\tan(p)$, where p is the phase to be added by the compensator to the frequency ω_{BW}. Also calculate $c=10^{M/20}$.
(7) Starting from *delta*, c and $\omega_c=\omega_{BW}$, *obtain*α_i, τ_i, α_e and τ_e with (11).

3. TOOLBOX LEAD-LAG CONTROL

The CAD tool was developed with the Toolbox App Designer of ®Matlab. This tool incorporates the method described in Subsection 2.5. It has two graphical interfaces: the first called <<Menu>> and the second <<Cont-At-Ad>> (Fig. 3). <<Menu>> prompts the user for the converter parameters (data from Table 2), specifications of the desired step responses for the inner and outer loops (M_p, t_s, e_{ss}), the simulation time and the reference

$U(s)$. With the maximum voltage ripple $DeltaV$ in Fig. 3 the tool provides the minimum values to choose of C and L to maintain the continuous conduction mode Sira-Ramirez and Silva-Ortigoza (2006). The <<Cont-At-Ad-Ad>> interface is invoked from the top left corner of the <<Menu>> interface. In the tool area, the type of controller is selected, in this case internal (G_{ci}) or external (G_{cv}) lead-lag controller (other controllers will be incorporated in later work). The tool displays the simulation results, the value of the maximum current i_L and the output power of the converter. Four graphs are provided:

- Graph No 1: Displays the frequency response of the inner loop and of the outer loop.
- Graph No 2: Displays the frequency response of G_{ci} and G_{cv}, as well as the value of the parameters c, p, $delta$, ω_{BW} and MF.
- Graph No. 3: Displays the step response of the inner loop and the outer loop, as well as the value of the parameters K_{int}, α_i, τ_i, K_{ext}, α_e y τ_e, t_s y M_p.
- Graph No. 4: Display the control signals of the inner and outer loops.

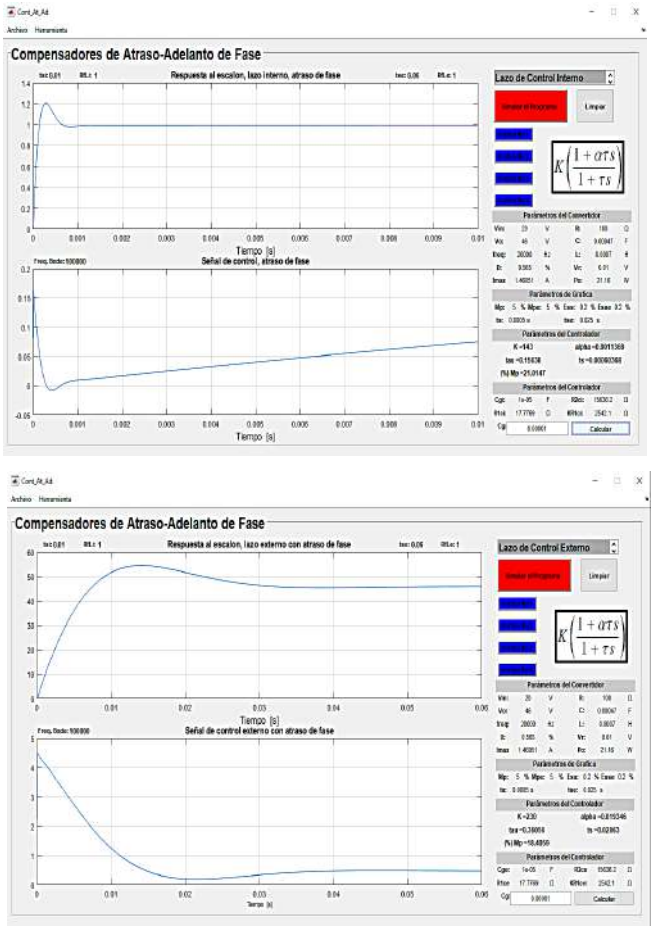


Fig. 3. Cont-At-Ad Graphical Interface.

4. RESULTS

The prototype Boost DC-DC converter was designed and simulated with the Toolbox lead-lag control from the specifications in Table 2:

Table 2. Design parameters of the CD-CD Boost converter 1.

Parameter	Value
Input voltage (V_in)	20V
Output voltage (V_o)	46V
Power output (P_o)	17.6W
Load resistor (R)	100 Ohm
Capacitor (C)	470μF
Inductor (L)	0.7mH
Switching frequency (F_s)	20KHz
Duty cycle (D)	56.5%

Inner loop: To obtain $G_{ci}(s)$ one has:

(1) Specifications: M_p<5%, t_s=0.5ms, e_{ss}<0.2%.
(2) These specifications result in: ξ=0.6901 y MF=64.63^o.
(3) From t_s and ξ we calculate: ω_{BW}=11871rad/s.
(4) With e_{ss}=0.2% result K_n=499. Since $G_{id}(0)$=3.5, K=143 is chosen.
(5) From the Bode diagram of $K \cdot Gid(s)$ we obtain F=$-$90.0443^o and $-M$=$-$58.0057dB at ω_{BW}=11871rad/s.
(6) p=$-$25.3257^o, δ=$-$0.4732 y c=0.0013 are calculated.
(7) With (8) and (11) are obtained:

$$G_{ci}(s) = \frac{0.02542s+143}{0.1564s+1} \tag{14}$$

The Fig. 4 shows the inner loop step response obtained with the Toolbox lead-lag control. Frequency and unit step responses were obtained that validate the design calculations. An overshoot of 21% was observed, higher than the expected 5% but within the range of other studies Karanjkar et al. (2012), and a settling time of 6ms, close to the specified 5ms. The initial control signal was less than 0.35V, suitable for OpAmps implementations.

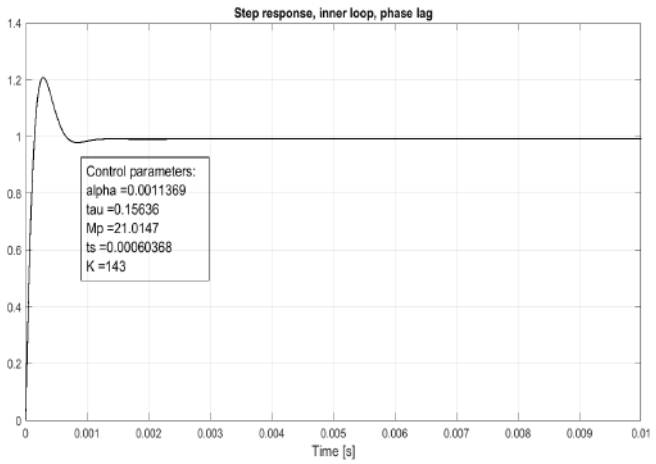


Fig. 4. Response to the inner loop step

Outer loop: To obtain $G_{cv}(s)$ one has:

(1) Specifications: M_p<5%, t_s=25ms, e_{ss}<0.2%.

(2) These specifications result in: ξ=0.6901 and MF=64.63^o.
(3) From t_s and ξ we calculate: ω_{BW}=237.42rad/s.
(4) With e_{ss}=0.2% result K_n=499, and given that $K_{LI}(0)$=2.2 K=230 is chosen.
(5) From the Bode diagram of $K \cdot K_{LI}(s)$ we obtain F=-84.9^o y $-M$=$-32.92dB$ at the ω_{BW}=237.42rad/s frecuency.
(6) p=-30.4576^o, δ=-0.5880 y c=0.0226 are calculated.
(7) With (8) and (11) result:

$$G_{cv}(s) = \frac{1.604s+230}{0.3606s+1} \tag{15}$$

The Fig. 5 illustrates the outer loop step response, where the Toolbox lead-lag control was re-run, obtaining frequency and unit step responses for the outer loop, validating the design calculations. An overshoot of 15.45% was observed, higher than the expected 5% but within the range of other studies Karanjkar et al. (2012), a settling time of 39ms, higher than the specified 25ms, and Fig. 5 shows an initial control signal of less than 3.5V, suitable for implementations with OpAmps.

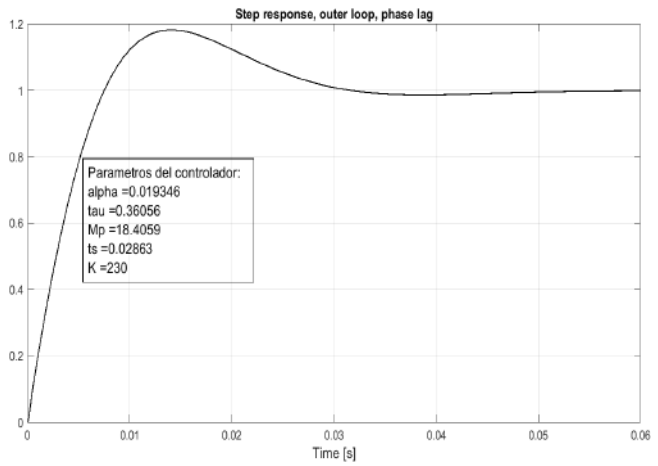


Fig. 5. Response to the outer loop step

In Fig. 6, the transient response of the converter to a step signal is shown. It is observed that the steady state voltage reaches values of 45.6V, 36.8V and 69V, corresponding to an overshoot of 15.45%. This value exceeds the anticipated 5%; however, it is within the range of results documented in previous research, as indicated in reference Karanjkar et al. (2012).

Additionally, Fig. 7 shows the control signal generated by $G_c v(s)$, which corroborates the calculations made during the design phase. An initial control signal of less than 3.5V is evident, a value that is within the standard operating range for implementations using operational amplifiers'.

In Fig. 8, the physical realisation of the prototype, which incorporates full-order phase delay controllers, is illustrated. The implementation was carried out using standard off-the-shelf discrete components and TL084 operational amplifiers, the latter powered with a ±5V voltage. The components of the on-board implementation are detailed, as well as the control circuit, which was assembled on an experimental board separate from the

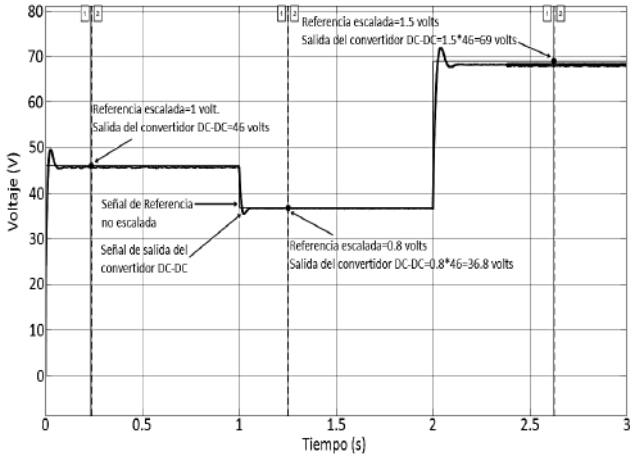


Fig. 6. Tracking at different voltage reference levels

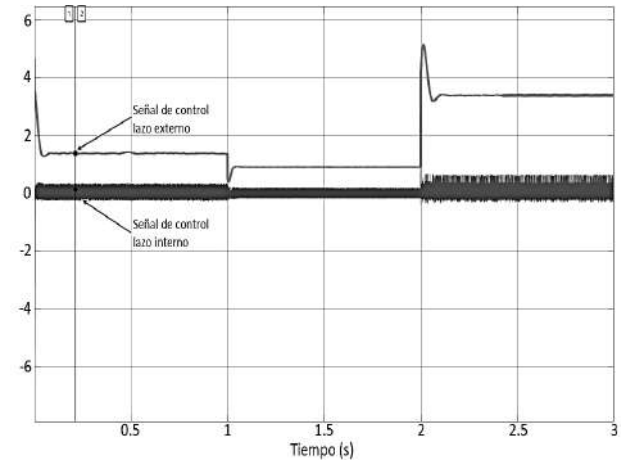


Fig. 7. Control loop signals G_{ci} and G_{cv}

DC-DC converter board. This arrangement facilitated the transition to the digital implementation. For characterisation, the experimental setup shown in Fig. 9 was used, which includes a Teledyne LeCroy Waverunner HD4096 oscilloscope, two Rigol DP83 DC power supplies - one of which is dedicated to generating the reference signal - a Fluence UT61E digital multimeter, and the control board previously mentioned in Fig. 8.

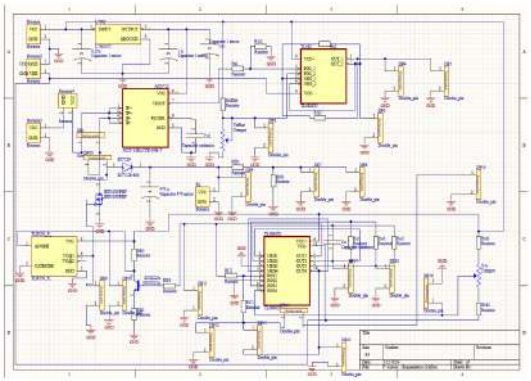
From Fig. 10, the step response of the implemented converter is shown, with M_p=8.6% and t_s=61.2ms; this time is higher than the design time of 25ms and the simulated time of 39ms, but the rise time of the reference signal of 24ms must be taken into account, so the resulting time of $62ms - 24ms = 37.2ms$ is consistent with the simulation results. Also, this step signal has a steady state voltage of 45.24V, which corresponds to a steady state error of 1.6% attributable to the tolerance of the passive electrical components. Note also that, despite the high noise content induced in the reference signal, the controller stabilises the output in the range of $\pm 0.5V$.

5. CONCLUSION

This paper highlights the relevance of the Toolbox lead-lag controller in the field of engineering, particularly in

power electronic systems. A Boost power converter was implemented using the Control lead-lag Toolbox. One of the advantages of this Toolbox in MATLAB is its focus on the design of phase lead-lag controllers. The approach proposed by (Wang) simplifies the application of control methodologies proposed by (Muniz-Montero), avoiding more complex techniques and automating the design of controllers for boost converters in power electronics systems.

(a)



(b)

Fig. 8. Implementation of the DC-DC Boost converter, a)Educational development card. b)Electronic diagram of the implementation.

Fig. 9. Experimental setup to characterise the Boost DC/DC converter: (1) Teledyne LeCroy Waverunner HD4096 oscilloscope; (2) Rigol DP83 DC power supplies; (3)Fluence UT61E digital multimeter; (4) Control board

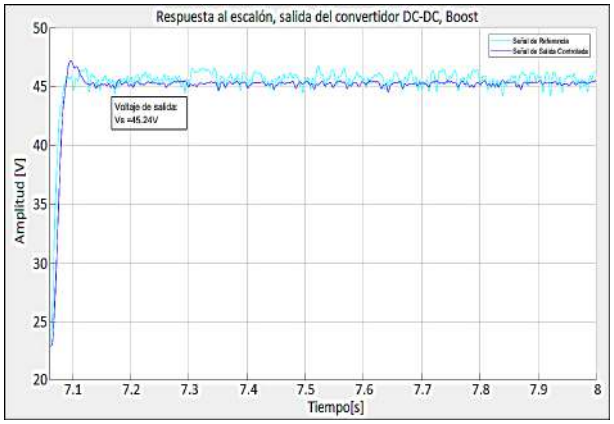


Fig. 10. Step response of the DC/DC converter type Boost.

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