

CMOS power upconverter with low power consumption suitable for UWB-IR in intra-vehicular wireless communications and VWSNs ^{*}

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Abstract: The design of a power upconverter with low power consumption in a six metal layers, 180nm CMOS technology from UMC foundry is presented. The proposed circuit is highly linear, exhibiting an IIP3 of 13.55dBm, a conversion factor of -5.6dB, a consumption of 45.48 μ W and a 3GHz bandwidth ranging from 3GHz to 6GHz. These features make the proposal suitable for UWB-IR transmission in intra-vehicular wireless communications and vehicular wireless sensor networks (VWSNs).

Keywords: UWB-IR, upconverter, CMOS, low power consumption.

1. INTRODUCTION

Ultra-Wide Band Impulse Radio (UWB-IR) makes use of radio frequency (RF) pulses with very short duration in order to carry the baseband (BB) information [Benedetto (2006), Darif et al. (2014)]. Compared to narrowband systems, the requirements on circuit blocks for Ultra-Wide Band transceivers (TRXs) are more challenging since performance demands such as bandwidth, noise figure (NF), gain, impedance matching and linearity are difficult to accomplish [Molnar et al. (2012)]. In case of transmitters, the most important performance features are gain, power consumption and linearity [Gaspariano et al. (2014)]. An abundant amount of publications regarding UWB-IR transmitter topologies can be found in the literature [Maduranga et al. (2014)], from conventional homodyne architectures to all-digital solutions. The latter of these being one of major interest in recent years due to its feasibility for CMOS realization with very few off-chip elements [Terada et al. (2005)]. However, the direct-up architecture still remains the dominant choice in state-of-the-art transmitters (TXs) [Mak and Martins (2009)] due to its integrability and low power. In-car wireless

communications face a dense multi-path data environment; nevertheless, the features of UWB-IR assure robust operation in intra-vehicular applications [Krészes et al. (2017)]. Moreover, the extremely short pulse durations keep the probability of message collision very low even in an ad-hoc network. These properties make UWB-IR an optimal technology for intra-vehicular wireless communications and VWSNs [Demir et al. (2014)].

Frequency translation of the BB spectrum to the RF frequency in direct-up transmitters is performed in one step by an upconversion mixer that usually precedes a power amplifier (PA) in the transmitter chain. Key aspects in the upconversion mixer should then deliver a sufficient power level to drive the PA and control the conduction angle of its output waveform. The concerns entailed between the interface of mixers and PAs are mainly focused in the ability of the former for driving the input capacitance of the latter, and the conversion of the differential waveforms from the mixer into a single-ended signal at the input of the amplifier. Such a practice is appropriate in wireless transmitters where the output power requirement is high as whenever it is necessary to add up more power gain, the use of a PA driver as the interceder between the upconversion mixer and the PA can be established. However, some wireless technologies demand a smaller output power, such is the case of UWB-IR. As the upconverter can drive directly to the antenna

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[Gaspariano et al. (2014)], the output power regulation can be included within the performance metrics of the mixer.

Recently, an alternative approach for UWB-IR by means of a mono-bit quantizer $\Sigma\Delta$ direct-up TX has been proposed [Shrestha et al. (2006)]. The system consists of a Continuous Time (CT) $\Sigma\Delta$ modulator, a Power Upconverter (PUC) with its corresponding Local Oscillator (LO), and a Bandpass Filter (BPF) before the antenna. At BB the adopted $\Sigma\Delta$ modulation converts the bit-stream into an encoded bit-stream with a reduced pulse density which alleviates the transmission power of the TX [Gaspariano et al. (2014)]. Then, at the RF section the PUC translates the BB to the corresponding UWB channel allocation at the same time as it drives the antenna. In sum, the proposal is a compact and simple solution. However, its feasibility is still unassessed since simulations at system level with the aid of Simulink RF Blockset are the only results reported.

The present work focuses in the design of a PUC for the Mono-Bit Quantizer $\Sigma\Delta$ TX for UWB-IR. The design of the circuit was made with the UMC 0.18 μm mixed mode/RF CMOS technology. Simulation results at post-layout level include: a third order input intercept point (IIP₃) of 13.55 dBm, a power consumption of 45.4 μW and a conversion factor (CF) of -5.6 dB.

The paper is organized as follows: section 2 describes the circuit design of the proposed CMOS PUC in a six metal layer, mixed mode/RF, 0.18 μm CMOS technology from the UMC foundry; on section 3, simulation results at post-layout level are discussed; finally, conclusions are drawn in section 4.

2. CMOS UP CONVERTER WITH LOW POWER CONSUMPTION SUITABLE FOR UWB-IR IN INTRA-VEHICULAR COMMUNICATIONS AND VWSNS

Fig. 1 shows the schematic diagram of the proposed PUC. As can be seen, it consists of a differential pair composed by transistors M_1 and M_2 where the BB signal is fed in differential mode. The BB signal is an encoded bit-stream generated by a $\Sigma\Delta$ modulator. The design of the $\Sigma\Delta$ modulator at transistor level is not considered in this work; instead, a behavioural $\Sigma\Delta$ modulator with Verilog-A is used. The power supply, V_{DD} , is delivered to the drain of M_1 and M_2 through the choke coils L_1 and L_2 , respectively. These inductors are not planar inductors from the CMOS process of the active devices but the bond-wires for the interconnection of the integrated circuit with its packaging. As mentioned earlier, a mixed mode/RF, 0.18 μm CMOS process from UMC foundry is employed in the design of the proposal. One of the features this technology has is the availability of planar inductors with a high quality factor on the thicker top copper metal. However, these inductors are better suited for the realizations of impedance-matching networks and resonant circuits such as oscillators. In

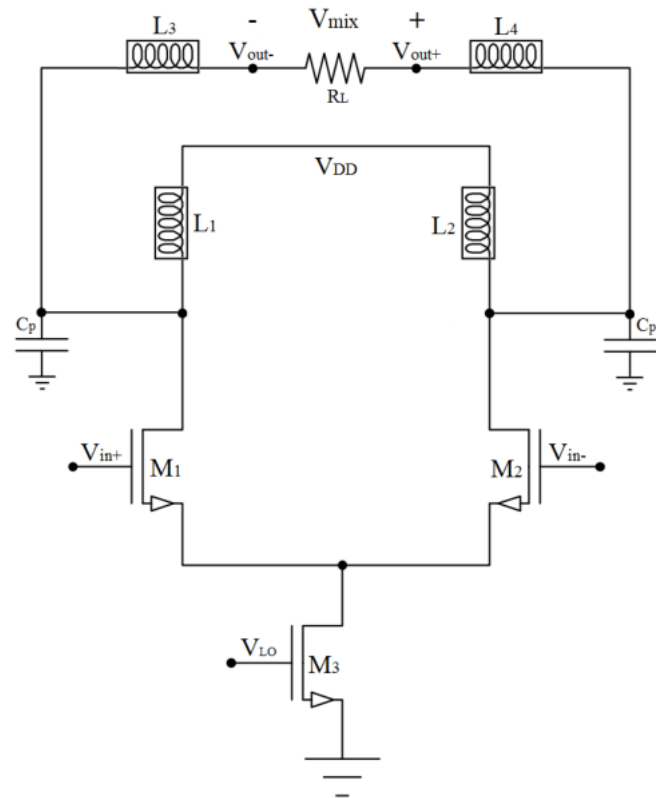


Fig. 1. Schematic diagram of the proposed mixer.

the case of our circuit, the purpose of L_1 and L_2 is to pass DC, while blocking or "choking off" the flow of RF currents to and from the supply, and to this end bond-wires are better [Bautista et al. (2017 A)]. Additionally, bond wires L_3 and L_4 are occupied to connect the circuit to the antenna of the TX, whose impedance in the band of interest is represented by R_L and has a value of $\sim 100\Omega$. The equivalent circuit of the bond-wire is shown in Fig.2, where C_B is the parasitic capacitance and for the CMOS process employed here has a value of 242 fF ; furthermore, $L_B = 5.8$ nH is the inductance of the wire. Capacitances C_p placed between the drain of $M_{1,2}$ and ground, respectively, represent the parallel of the parasitic capacitances of the bond-wires, the parasitic capacitances of M_1 and M_2 , and the capacitance of the output pads, which have a value of 50 fF each.

Transistor M_3 is switched from off to the linear region by the LO signal. When LO turns off M_3 , there is not a DC path from V_{DD} to ground and thus the differential pair does not produce an output waveform even though there is an input stimulus. Conversely, when LO turns on M_3 this transistor behaves like a low ohmic resistor and consequently the differential pair acts like an emitter degenerated amplifier whose voltage gain is approximately given by gmR_L , where gm is the transconductance of the differential pair M_1 and M_2 , and R_L is the ohmic value of the antenna. It can be proved that the output signal of the circuit is given by [Gaspariano et al. (2014)]:

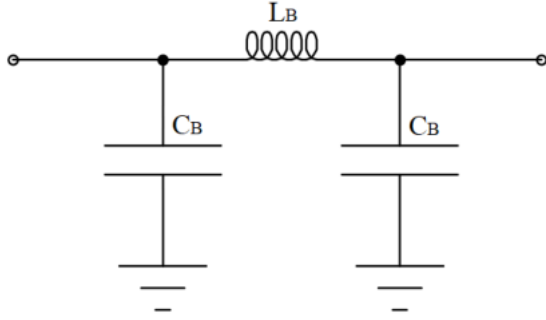


Fig. 2. Schematic diagram of the bond-wires.

$$\begin{aligned}
 v_{mix}(t) = & \frac{A}{2} \cos((\omega_{lo} - \omega_b)t) - \frac{A}{2} \cos((\omega_{lo} + \omega_b)t) \\
 & + \frac{A}{6} \cos((\omega_{lo} - 3\omega_b)t) - \frac{A}{6} \cos((\omega_{lo} + 3\omega_b)t) \\
 & + \frac{A}{10} \cos((\omega_{lo} - 5\omega_b)t) - \frac{A}{10} \cos((\omega_{lo} + 5\omega_b)t) \\
 & + \frac{A}{6} \cos((3\omega_{lo} - \omega_b)t) - \frac{A}{6} \cos((3\omega_{lo} + \omega_b)t) \\
 & + \frac{A}{18} \cos((3\omega_{lo} - 3\omega_b)t) - \frac{A}{18} \cos((3\omega_{lo} + 3\omega_b)t) \\
 & + \frac{A}{30} \cos((3\omega_{lo} - 5\omega_b)t) - \frac{A}{30} \cos((3\omega_{lo} + 5\omega_b)t) \\
 & + \frac{A}{10} \cos((5\omega_{lo} - \omega_b)t) - \frac{A}{10} \cos((5\omega_{lo} + \omega_b)t) \\
 & + \frac{A}{30} \cos((5\omega_{lo} - 3\omega_b)t) - \frac{A}{30} \cos((5\omega_{lo} + 3\omega_b)t) \\
 & + \frac{A}{50} \cos((5\omega_{lo} + 5\omega_b)t) - \frac{A}{50} \cos((5\omega_{lo} - 5\omega_b)t)
 \end{aligned} \quad (1)$$

where ω_{lo} is the frequency of the carrier provided by the LO, ω_b is the baseband frequency that comes from the $\Sigma\Delta$ modulator, and A is the amplitude of the fundamental frequency of the Fourier series.

Thus, both the upper and lower sided terms are preserved around the fundamental and harmonics of LO. Since LO runs at a high frequency, the terms are allocated far from each other; consequently the output spectrum can be shaped by a low order filter.

The power consumption of the circuit is given by the product of the transconductance related to $I_{dM_{1,2}}$ and the power supply V_{DD} . Therefore, it is proportional to the size of these devices. Since the output power demanded by the UWB-IR standard is rather small, M_1 and M_2 are small as well and consequently, the circuit has a low DC consumption, desirable for UWB-IR applications.

3. CIRCUIT DESIGN

The circuit was dimensioned in accordance to the method used by Mensink[Shresta et al. (2006)], which choses the width of the transistors in order to maximize the circuit amplification while making transistor width as small as

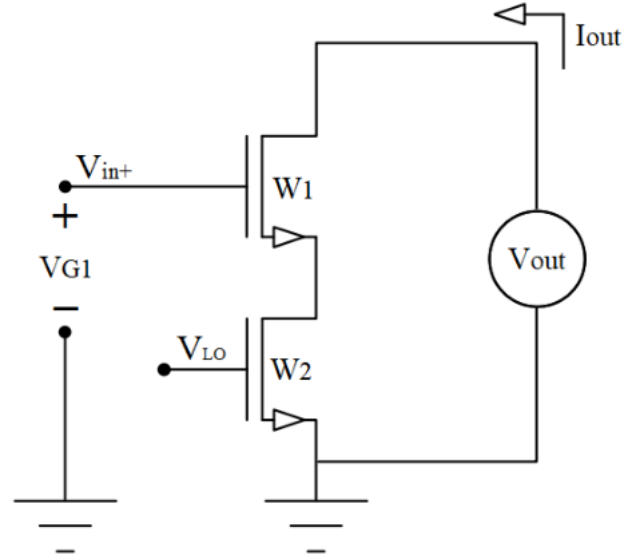


Fig. 3. Schematic used to calculate the width of the transistors.

possible. This means that the sum of the widths of all three transistors is as small as possible and the total silicon area is reduced. The schematic shown in Fig. 3 is used in order to calculate the width of the transistors. We assume an ideal load, therefore a voltage source is used.

The transconductance G_m needed for calculations is determined by:

$$G_m = \frac{\delta I_{out}}{\delta V_{G1}} \quad (2)$$

Both terms can be obtained from the CMOS transistor current equation:

$$I_{out} \approx \frac{1}{2} \mu C_{ox} \frac{W_1}{L} (V_{GS1} - V_{TH})^2 \quad (3)$$

Where V_{G1} is the voltage level in the gate of the upper transistor and W_1 is the transistor width. As both transistors share the same channel length this is noted as L . V_{GS1} in this expression can be expanded as:

$$V_{GS1} = V_{G1} - R_{sw} I_{out} \quad (4)$$

Where R_{sw} represents the resistance of the lower transistor which serves as a switch. When the transistor is off, R_{sw} is expected to be very large and $G_m \approx 0$. When the transistor is on, we obtain:

$$R_{sw} \approx \frac{1}{\mu C_{ox} \frac{W_2}{L} (V_{GS2} - V_{TH})} \quad (5)$$

Combining equations 3, 4 and 5 results in:

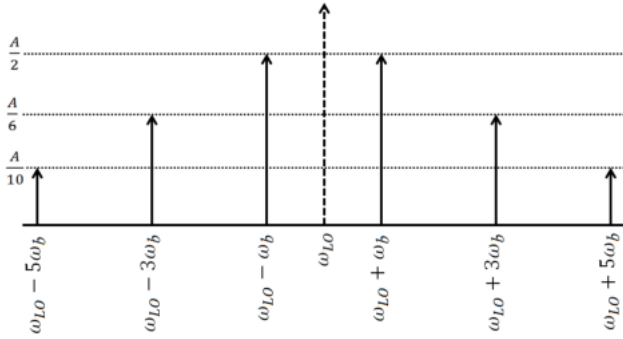


Fig. 4. Distribution of most significant harmonics in the system. LO is marked as a dotted line.

$$I_{out} \approx \frac{1}{2} \mu C_{ox} \frac{W_1}{L} (V_{G1} - \frac{I_{out}}{\mu C_{ox} \frac{W_2}{L} (V_{GS2} - V_{TH})} - V_{TH})^2 \quad (6)$$

Solving for 6 the values for transistor width and length can be determined after selecting desired values. Maximum power excursion is obtained when $W_1 = W_2$, so values are determined accordingly. It should be noted that when the circuit is in differential mode, the total width obtained for W_1 is divided by two for M_1 and M_2 . In order to accomplish the UWB-IR transmission requirements and considering losses of around 40%, the transistor dimensions obtained in the proposed circuit are 900 nm/270 nm for M_1 and M_2 and 1.8 μm /270 nm for M_3 .

To verify the functionality of the circuit as a mixer, a behavioural simulation was carried out. Fig.4 shows the achieved spectrum. The LO component is dotted since it is theoretically cancelled. According to this result, and since A is a low power value (~ -38 dBm including losses), expression (1) can be reduced to:

$$v_{mix}(t) = \frac{A}{2} \cos((\omega_{lo} - \omega_b)t) - \frac{A}{2} \cos((\omega_{lo} + \omega_b)t) + \frac{A}{6} \cos((\omega_{lo} - 3\omega_b)t) - \frac{A}{6} \cos((\omega_{lo} + 3\omega_b)t) + \frac{A}{10} \cos((\omega_{lo} - 5\omega_b)t) - \frac{A}{10} \cos((\omega_{lo} + 5\omega_b)t) \quad (7)$$

Fig.5 shows the layout of the proposal, realized in Cadence IC6.1.6.101 Virtuoso design environment with a six metal layers, 180 nm CMOS technology from UMC foundry. As can be seen, the length of all transistors is 270 nm, whereas the widths are 900 nm for $M_{1,2}$ and 1.8 μm for M_3 . As RF transistors emanate a large amount of energy, two guard rings are included around each transistor in order to prevent crosstalk between them.

Note that due to the use of bondwires, the only on-chip components are transistors M_1 , M_2 , and M_3 . As M_3 has a multiplicity of 2, its total width is halved and as such has a width of 900 nm across its two transistor components.

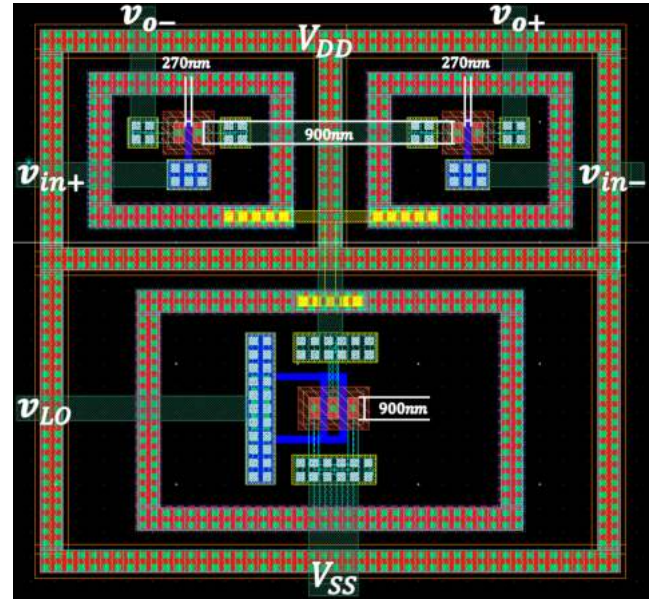


Fig. 5. Layout of the proposed mixer.

4. SIMULATION RESULTS

The circuit was simulated using the Cadence IC6.1.6.101 Spectre analog design environment with the UMC 0.18 μm technology mentioned earlier. A single tone test was realized using a baseband carrier frequency of $v_c = 500$ MHz and an LO frequency of $v_{LO} = 4$ GHz to realize frequency translation. The LO signal ranges from 0 V to 1.8 V and from 3-6 GHz while the carrier signal ranges from 600 mV to 691.2 mV.

As regulations dictate that the circuit must have an output no greater than -40 dBm/MHz, it must be designed to fulfill this restriction. We consider possible loss from the fabrication process as well as parasitic components in the circuit packaging and set the circuit to output -38 dBm/MHz, 40% greater than the required -40 dBm/MHz set by the UWB standard. Fig.6 shows the power in frequency components close to the desired signal at 4.5 GHz. Note that the harmonic at 5 GHz is present but significantly reduced, meaning it is unlikely to affect the component of interest. Therefore it is the second harmonic at 5.5 GHz or the harmonic at 3.5 GHz that might affect this signal. However, since this component is far from the main signal and has a lower magnitude, it is easy to suppress. The entire mixer consumes a total of 17.92 μW .

Voltage and power conversion are -5.6 dB and -2.8 dB respectively. As the baseband signal is intended to come from a $\Sigma\Delta$ modulator and the output is designed for use in UWB standard, a loss in conversion is expected in order to remain within regulations.

Mixer linearity was obtained by sweeping signal power excursion from -80 dBm to 30 dBm for the desired signal at 4.5 GHz and the harmonic at 5.5 GHz. Results show that the circuit is highly linear, with an IIP3 of 13.55 dBm. This can be appreciated in Fig.7.

Table 1. Comparison of several UWB TX

	This work	Kassiri (2013)	Pasca (2013)	Murad (2010)	Wu (2010)	Bautista (2017 B)
Technology	0.18 μm	0.13 μm	65 nm	0.18 μm	0.18 μm	0.18 μm
RF Frequency	4.5-6 GHz	3.1-10.6 GHz	4.5-8 GHz	3-5 GHz	3-5 GHz	3.1-10.6 GHz
LO Frequency	4-6 GHz	7.5 GHz	4.5 GHz	2.9-4.9 GHz	6.5 GHz	772.5 MHz
BB Frequency	500 MHz	-	0 Hz	-	-	10 MHz
Power Supply	1.8 V	1.2 V	1.2 V	1.2 V	1.2 V	1.8 V
Power consumption	45.4 μW	620 μW	2.4-2.7 mW	7.1 mW	7.2 mW	11.85 mW
Conversion factor	-5.6 dB	14.9 dB	4-2 dB	2.3 dB	12.38-15.69 dB	-6.63 dB
IIP3	13.55 dBm	9.2 dBm	12-11.8 dBm	9.8-13.5 dBm	-5-1.64 dBm	16.26 dBm

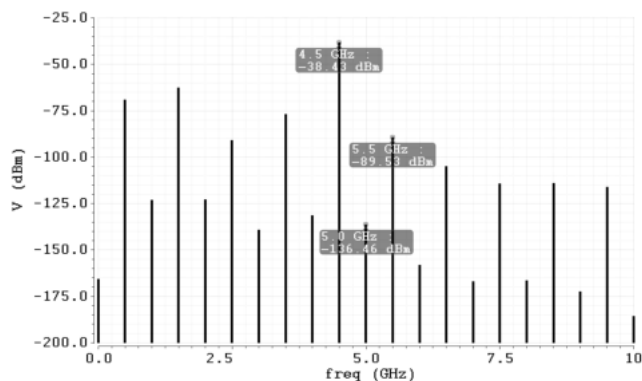


Fig. 6. Power excursion at circuit output.

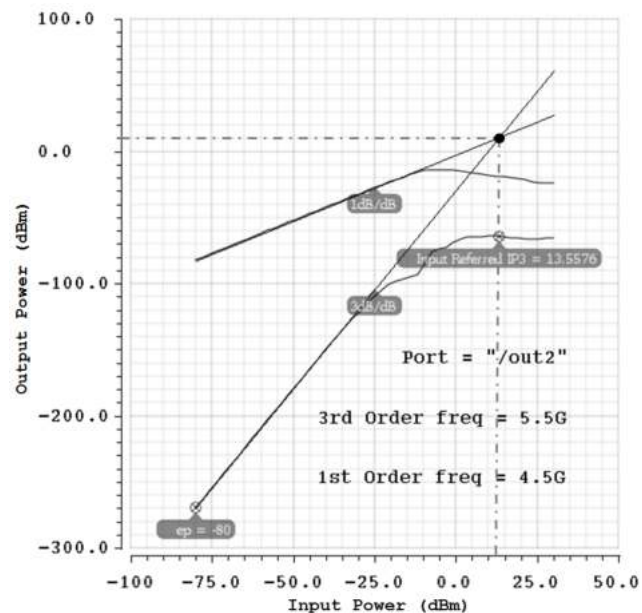


Fig. 7. IIP3 of the proposed mixer.

The obtained simulation results are summarized and compared to other works in Table.1. Compared to other proposals, the suggested circuit architecture exhibits the lowest power consumption, which makes it profitable for in-car communications and VWSNs.

5. CONCLUSION

The design for a CMOS power upconverter which consists only of three transistors and is suitable for UWB applications was realized. In order to reduce active silicon area the system uses bondwires as mixer loads. The main contribution of this work lies in the fact that the system complies with the required power emission for UWB standard and consumes 45.4 μW . Conversion gain for the circuit stands at around -5.6 dB. Due to the use of a differential architecture, nearby harmonics are greatly reduced, resulting in an IIP3 of 13.55. Results show potential for use in the UWB frequency band.

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